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ABSTRACT:
PROBLEM TO BE SOLVED: To reduce **contact** resistance in the impurity diffused region of a MOSFET by forming an **etching stopper film after selectively** removing the sidewall **spacers** formed on the side surfaces of its **gate** electrode.

SOLUTION: After selectively removing the sidewall **spacers** formed on the side surfaces of a **gate** electrode 5, an etching stopper film 10 is formed. As a result, when by applying an anisotropic etching to an interlayer insulating film 11 and the etching stopper film 10, a **contact hole** 12 for diffused regions is formed on a heavily-doped diffused region 9 present between the **gate** electrode 5 and an element isolation region 3 of a semiconductor substrate 1, and the distance between the etching stopper film 10 remaining on the side surface of the **gate** electrode 5 and the element isolation region 3 of the semiconductor substrate 1 can be made large. Therefore, the bottom area of the **contact hole** 12 for diffused regions can be increased to reduce the **contact** resistance in the heavily-doped diffused region 9.

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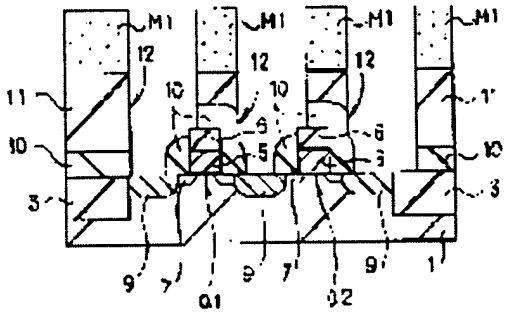
(54) MANUFACTURE OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce contact resistance in the impurity diffused region of a MOSFET by forming an etching stopper film after selectively removing the sidewall spacers formed on the side surfaces of its gate electrode.
SOLUTION: After selectively removing the sidewall spacers formed on the side surfaces of a gate electrode 5, an etching stopper film 10 is formed. As a result, when by applying an anisotropic etching to an interlayer insulating film 11 and the etching stopper film 10, a contact hole 12 for diffused regions is formed on a heavily-doped diffused region 9 present between the gate electrode 5 and an element isolation region 3 of a semiconductor substrate 1, and the distance between the etching stopper film 10 remaining on the side surface of the gate electrode 5 and the element isolation region 3 of the semiconductor substrate 1 can be made large. Therefore, the bottom area of the contact hole 12 for diffused regions can be increased to reduce the contact resistance in the heavily-doped diffused region 9.



* NOTICES *

CLAIMS [Claim(s)]
[Claim 1] The above MISFET is the manufacture method of the semiconductor integrated circuit equipment which has MISFET to the element formation field of the semiconductor substrate characterized by to provide the following, and has the composition of having the gate electrode by which the upper surface was being worn by the cap insulator layer, and the side was being worn with the sidewall spacer, the low-concentration impurity-diffusion field formed by self-adjustment to the aforementioned gate electrode, and the high-concentration impurity-diffusion field formed by self-adjustment to the aforementioned sidewall spacer. The process which removes the aforementioned sidewall spacer alternatively, forms the etching stopper film which has selectivity to a ground on the aforementioned semiconductor substrate as covers the aforementioned cap insulator layer after that, and forms after that the layer insulation film which has selectivity to it on the aforementioned etching stopper film. the contact which gives anisotropic etching on the conditions which can take a selection ratio to the aforementioned etching stopper film on the aforementioned layer insulation film, gives anisotropic etching after that on the conditions which can take a selection ratio to the ground on the aforementioned etching stopper film, and arrives at the aforementioned high concentration impurity diffusion field from the aforementioned layer insulation film -- the process which forms a hole
[Claim 2] It has each of the first MISFET and the second MISFET to the element formation field of the semiconductor substrate characterized by providing the following. each of the first above MISFET and the second MISFET The gate electrode by which the upper surface was being worn by the cap insulator layer, and the side was being worn with the sidewall spacer, The low concentration impurity diffusion field of the couple formed by self-adjustment to the aforementioned gate electrode, It has the composition of having the high concentration impurity diffusion field of the couple formed by self-adjustment to the aforementioned sidewall spacer. The first above MISFET and each gate electrode of the second MISFET are arranged in parallel, and one high concentration impurity diffusion field of the first above MISFET is gate inter-electrode [aforementioned]. The process which is the manufacture method of the semiconductor integrated circuit equipment currently shared with one high-concentration impurity-diffusion field of the second above MISFET, removes the aforementioned sidewall spacer alternatively, forms the etching stopper film which has selectivity to a ground on the aforementioned semiconductor substrate as covers the aforementioned cap insulator layer after that, and forms after that the layer-insulation film which has selectivity to it on the aforementioned etching stopper film. the contact which gives anisotropic etching on the conditions which can take a selection ratio to the aforementioned etching stopper film on the aforementioned layer insulation film, gives anisotropic etching after that on the conditions which

can take a selection ratio to the ground on the aforementioned etching stopper film, and arrives at the aforementioned high concentration impurity diffusion field from the aforementioned layer insulation film -- the process which forms a hole

[Claim 3] The above MISFET is the manufacture method of the semiconductor integrated circuit equipment which has MISFET to the element formation field of the semiconductor substrate characterized by to provide the following, and has the composition of having the gate electrode by which the upper surface was being worn by the cap insulator layer, and the side was being worn with the sidewall spacer, the low-concentration impurity-diffusion field formed by self-adjustment to the aforementioned gate electrode, and the high-concentration impurity-diffusion field formed by self-adjustment to the aforementioned sidewall spacer. The process which removes the aforementioned sidewall spacer alternatively, forms the etching stopper film which has selectivity to a ground on the aforementioned semiconductor substrate as covers the aforementioned cap insulator layer after that, and forms after that the layer insulation film which has selectivity to it on the aforementioned etching stopper film. the contact which gives anisotropic etching on the conditions which can take a selection ratio to the aforementioned etching stopper film on the aforementioned layer-insulation film, gives anisotropic etching after that on the conditions which can take a selection ratio to the ground on the aforementioned etching stopper film, gives anisotropic etching after that on the conditions which can take a selection ratio to the aforementioned gate electrode and the aforementioned etching stopper film to the aforementioned cap insulator layer, and reaches the aforementioned gate electrode from the aforementioned layer-insulation film -- the process which forms a hole

[Claim 4] The aforementioned etching stopper film is the manufacture method of the semiconductor integrated circuit equipment according to claim 1 or 2 characterized by forming by thickness thicker than the width of face of the direction of gate length of the aforementioned sidewall spacer.

[Claim 5] It is the manufacture method of semiconductor integrated circuit equipment given in any or the first term among the claim 1 characterized by forming the aforementioned cap insulator layer by the silicon-oxide film, and forming each of the aforementioned sidewall spacer and the aforementioned etching stopper film by the silicon nitride film, or a claim 3.

[Translation done.]

DETAILED DESCRIPTION [Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention is applied to the semiconductor integrated circuit equipment which has MISFET (Metal Insulator Semiconductor Field Effect Transistor) of LDD (Lightly Doped Drain) structure about semiconductor integrated circuit equipment, and relates to effective technology.
[0002]
[Description of the Prior Art] MOSFET (Metal Oxide Semiconductor Field Effect Transistor) accumulated by semiconductor integrated circuit equipment turns minutely with high integration, and adoption of the LDD structure where the portion by the side of the channel formation field of a drain field was set as low high impurity concentration compared with the high impurity concentration of other portions serves as indispensable requirements in MOSFET to which a gate-length size reaches submicron one especially. Since MOSFET of this LDD structure reduces the diffusing capacity by the side of the channel formation field of a drain field and can secure a channel-length size, it can suppress generating of a short channel effect. Moreover, MOSFET of LDD structure eases the inclination of the impurity atom concentration profile of the pn junction section formed between a drain field and a channel formation field, and since it can weaken the field strength generated to this field, it can suppress generating of a hot carrier effect.
[0003] by the way -- in order to attain high integration of semiconductor integrated circuit equipment -- detailed-izing, simultaneously " of a processing size -- a gate electrode and contact -- the doubling between each structure distance" between holes needs to be reduced an impurity diffusion field [which turns into a source field of MOSFET, and a drain field now using SAC (Self Aligned Contact hole) technology], and gate electrode top -- self-adjustment -- contact -- contact of as opposed to [form a hole and] the gate electrode of the isolation field of a semiconductor substrate or MOSFET -- reduction of the doubling margin of a hole is aimed at
[0004] About SAC technology, for example Eye I dee em 93[IEDM93, and p441 and A Novel Borderless Contact/Interconnect Technology Using Aluminum Oxide Etch Stop for High Performance It is indicated by SRAM and Logic].
[0005]
[Problem(s) to be Solved by the Invention] the SAC technology after forming MOSFET of LDD structure -- using -- contact -- the trouble in the case of forming a hole is explained using drawing 18 or drawing 22 (cross section for explaining the manufacture method)
[0006] First, a slot 22 is formed in the isolation field of the principal plane of a silicon substrate 21, after that, in a slot 22, the insulator layer 23 for isolation which consists of a silicon-oxide film is embedded, and between the element formation fields of the principal plane of a silicon

substrate 21 is separated electrically.
[0007] Next, as shown in drawing 18 , MOSFET-Q4 of LDD structure and MOSFET-Q5 of LDD structure are formed in the element formation field of a silicon substrate 21. Each of MOSFETQ4 and Q5 has the composition of mainly having the silicon substrate 21 used as a channel formation field, the gate insulator layer 24 which consists of a silicon-oxide film, the gate electrode 25 which consists of a polycrystal silicon film, the low concentration impurity diffusion field 27 of a couple used as a source field and a drain field, and the high concentration impurity diffusion field 29 of a couple used as a source field and a drain field. The gate electrode 25 is covered by the cap insulator layer 26 which the upper surface becomes from a silicon-oxide film, and is covered with the sidewall spacer (side-attachment-wall insulator layer) 28 with which the side (side attachment wall) consists of a silicon-oxide film. The low concentration impurity diffusion field 27 of a couple is formed by self-adjustment to the gate electrode 25, and the high concentration impurity diffusion field 29 of a couple is formed by self-adjustment to the sidewall spacer 28. Each gate electrode 25 of MOSFETQ4 and Q5 is arranged in parallel. One high concentration impurity diffusion field 29 of MOSFETQ4 is shared with one high concentration impurity diffusion field 29 of MOSFETQ5.
[0008] Next, as are shown in drawing 19 , and the cap insulator layer 26 and the sidewall spacer 28 are covered, the etching stopper film 30 is formed the whole surface on a silicon substrate 21. The etching stopper film 30 is formed by the film which has selectivity to the silicon oxide of the insulator layer 23 for isolation, the cap insulator layer 26, and sidewall spacer 28 grade, and the silicon of silicon-substrate 21 grade (it is the film which can be etched alternatively), for example, a silicon nitride film.
[0009] Next, the layer insulation film 31 is formed on the etching stopper film 30. The layer insulation film 31 forms the film (it is the film which can be etched alternatively) and metaphor of having selectivity to the etching stopper film 30, by the silicon-oxide film.
[0010] next, each high concentration impurity diffusion field 29 top of MOSFETQ4 and Q5 -- the contact for diffusion fields -- the resist mask M3 for forming a hole is formed on the layer insulation film 31 using photolithography technology
[0011] Next, as the resist mask M3 is used as an etching mask and it is shown in drawing 20 Anisotropic etching is given to the layer insulation film 31 on the conditions which can take a selection ratio to the etching stopper film 30. Then, anisotropic etching is given to the etching stopper film 30 on the conditions which can take a selection ratio to the silicon oxide of the insulator layer 23 for isolation which is the ground of the etching stopper film 30, the cap insulator layer 26, and sidewall spacer 28 grade, and the silicon of silicon-substrate 21 grade. the contact for diffusion fields which arrives at the high concentration impurity diffusion field 29 from the front face of the layer insulation film 31 as shown in drawing 21 -- a hole 32 is formed
[0012] next -- although the resist mask M3 is removed and not being illustrated after that -- the contact for diffusion fields -- the contact for the gates which reaches the gate electrode 25 from the front face of the layer insulation film 31 using the same method as a hole 32 -- a hole is formed
[0013] next, the contact for diffusion fields -- the inside of a hole 32, and the contact for the gates -- a hole -- by being filled up with electric conduction objects, such as a metal, inside, forming the electric conduction plug 14 in it, and forming wiring 15 in it after that, as shown in drawing 22 , MOSFETQ4 and Q5 are alike, respectively, and the upper wiring 15 is connected electrically
[0014] the ** which will not affect the sidewall spacer 28 and the insulator layer 23 for isolation

if the above-mentioned method is used -- the contact for diffusion fields -- since a hole 32 can be formed -- the gate electrode 25 and the contact for diffusion fields -- the distance between holes 32 is reducible

[0015] however, since thickness looks thick in efficiency as anisotropic etching like the sidewall spacer 28 when the etching stopper film 30 is formed in a perpendicular portion to a silicon substrate 31, it is shown in drawing 21 -- as -- the contact for diffusion fields -- the etching stopper film 30 remains thickly in the shape of a side attachment wall by side of the sidewall spacer 28 by the anisotropic etching when forming a hole 32 for this reason, the contact for diffusion fields -- the low area (exposed-surface product of a high concentration impurity diffusion field) of a hole 32 contracts, and there is a problem that the contact resistance in the high concentration impurity diffusion field 29 between the isolation field (insulator layer 23 for isolation) of a silicon substrate 21 and the gate electrode 25 and the contact resistance in the high concentration impurity diffusion field 29 between the gate electrodes 25 increase

[0016] moreover, the element formation field top of a silicon substrate -- setting -- the contact for the gates -- the trouble in the case of forming a hole is explained using drawing 23 (cross section for explaining the manufacture method)

[0017] the gate electrode 25 top of MOSFET-Q6 -- the contact for the gates -- the resist mask M4 for forming a hole is formed on the layer insulation film 31 using photolithography technology

[0018] Next, use the resist mask M4 as an etching mask, and anisotropic etching is given to the layer insulation film 31 on the conditions which can take selectivity to the etching stopper film 30. Then, anisotropic etching is given to the etching stopper film 30 on the conditions which can take a selection ratio to the cap insulator layer 26 and the sidewall spacer 28. then, the contact for the gates which reaches from the upper surface of the layer insulation film 31 on the element formation field of a silicon substrate 21 at the gate electrode 25 by giving anisotropic etching to the cap insulator layer 26 on the conditions which can take a selection ratio to the gate electrode 25 -- a hole 33 can be formed

[0019] making the amount of over etching at the time of etching of the cap insulator layer 26 below into the thickness of the gate electrode 25, if the above-mentioned method is used -- the contact for the gates from the gate electrode 25 -- even if it is a case so that a hole 33 may overflow, without it exposes the low concentration impurity diffusion field 27 and the high concentration impurity diffusion field 29 -- the contact for the gates -- a hole 33 can be formed

[0020] however -- since the permissible amount of over etching has only a grade equivalent to the thickness of the gate electrode 25 -- the contact for the gates -- the gate electrode and impurity diffusion field which are produced through the electric conduction object (an electric conduction plug or a part of wiring) with which it filled up in the hole 33 -- simplistic -- the receiving margin is small

[0021] The purpose of this invention is to offer the technology which can reduce the contact resistance in the impurity diffusion field of MISFET.

[0022] other purposes of this invention -- the gate electrode of MISFET, and an impurity diffusion field -- simplistic -- it is in offering the technology which can enlarge the receiving margin

[0023] The other purposes and the new feature will become clear by description and the accompanying drawing of this specification at the aforementioned row of this invention.

[0024]

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly

explained among invention indicated in this application.
[0025] It has MISFET to the element formation field of a semiconductor substrate. (1) Above MISFET The gate electrode by which the upper surface was being worn by the cap insulator layer, and the side was being worn with the sidewall spacer, The low concentration impurity diffusion field formed by self-adjustment to the aforementioned gate electrode, It is the manufacture method of the semiconductor integrated circuit equipment which has the composition of having the high concentration impurity diffusion field formed by self-adjustment to the aforementioned sidewall spacer. Remove the aforementioned sidewall spacer alternatively and the etching stopper film which has selectivity to a ground on the aforementioned semiconductor substrate as covers the aforementioned cap insulator layer is formed after that. Then, the process which forms the layer insulation film which has selectivity to it on the aforementioned etching stopper film, Give anisotropic etching on the conditions which can take a selection ratio to the aforementioned etching stopper film on the aforementioned layer insulation film, and anisotropic etching is given after that on the conditions which can take a selection ratio to the ground on the aforementioned etching stopper film. the contact which arrives at the aforementioned high concentration impurity diffusion field from the front face of the aforementioned layer insulation film -- it has the process which forms a hole
[0026] It has each of the first MISFET and the second MISFET to the element formation field of a semiconductor substrate. (2) Each of the first above MISFET and the second MISFET The gate electrode by which the upper surface was being worn by the cap insulator layer, and the side was being worn with the sidewall spacer, The low concentration impurity diffusion field of the couple formed by self-adjustment to the aforementioned gate electrode, It has the composition of having the high concentration impurity diffusion field of the couple formed by self-adjustment to the aforementioned sidewall spacer. The first above MISFET and each gate electrode of the second MISFET are arranged in parallel. one high concentration impurity diffusion field of the first above MISFET It is the manufacture method of the semiconductor integrated circuit equipment currently shared with one high concentration impurity diffusion field of the second above MISFET in the aforementioned gate inter-electrode. Remove the aforementioned sidewall spacer alternatively and the etching stopper film which has selectivity to a ground on the aforementioned semiconductor substrate as covers the aforementioned cap insulator layer is formed after that. Then, the process which forms the layer insulation film which has selectivity to it on the aforementioned etching stopper film, Give anisotropic etching on the conditions which can take a selection ratio to the aforementioned etching stopper film on the aforementioned layer insulation film, and anisotropic etching is given after that on the conditions which can take a selection ratio to the ground on the aforementioned etching stopper film. the contact which arrives at the aforementioned high concentration impurity diffusion field from the front face of the aforementioned layer insulation film -- it has the process which forms a hole
[0027] It has MISFET to the element formation field of a semiconductor substrate. (3) Above MISFET The gate electrode by which the upper surface was being worn by the cap insulator layer, and the side was being worn with the sidewall spacer, The low concentration impurity diffusion field formed by self-adjustment to the aforementioned gate electrode, It is the manufacture method of the semiconductor integrated circuit equipment which has the composition of having the high concentration impurity diffusion field formed by self-adjustment to the aforementioned sidewall spacer. Remove the aforementioned sidewall spacer alternatively and the etching stopper film which has selectivity to a ground on the aforementioned

semiconductor substrate as covers the aforementioned cap insulator layer is formed after that. Then, the process which forms the layer insulation film which has selectivity to it on the aforementioned etching stopper film, Anisotropic etching is given on the conditions which can take a selection ratio to the aforementioned etching stopper film on the aforementioned layer insulation film. Then, anisotropic etching is given on the conditions which can take a selection ratio to the ground on the aforementioned etching stopper film. then, the contact which gives anisotropic etching on the conditions which can take a selection ratio to the aforementioned gate electrode and the aforementioned etching stopper film to the aforementioned cap insulator layer, and reaches the aforementioned gate electrode from the front face of the aforementioned layer insulation film -- it has the process which forms a hole

[0028] By forming an etching stopper film, after removing alternatively the sidewall spacer formed in the side of a gate electrode according to the means (1) mentioned above Anisotropic etching is given to each of a layer insulation film and an etching stopper film. the high concentration impurity diffusion field top between a gate electrode and the isolation field of a semiconductor substrate -- contact, since the distance between the etching stopper films and the isolation fields of a semiconductor substrate which remain on the side of a gate electrode becomes large in case a hole is formed the contact in during this period -- the area of base (exposed-surface product of a high concentration impurity diffusion field) of a hole can be increased Consequently, the contact resistance in the high concentration impurity diffusion field of MISFET can be reduced.

[0029] By forming an etching stopper film, after removing alternatively the sidewall spacer formed in the side of a gate electrode according to the means (2) mentioned above Anisotropic etching is given to each of a layer insulation film and an etching stopper film. a gate inter-electrode high concentration impurity diffusion field top -- contact, since the distance between the etching stopper film which remains on the side of one gate electrode, and the etching stopper film which remains on the side of the gate electrode of another side becomes large in case a hole is formed the contact in during this period -- the area of base (exposed-surface product of a high concentration impurity diffusion field) of a hole can be increased Consequently, the contact resistance in the high concentration impurity diffusion field of MISFET can be reduced.

[0030] By forming the etching stopper film which has selectivity to a cap insulator layer, after removing alternatively the sidewall spacer formed in the side of a gate electrode according to the means (3) mentioned above the contact from a gate electrode, since the amount of over etching which can approve when **********ing a cap insulator layer serves as a grade equivalent to the thickness which added the cap insulator layer to the thickness of a gate electrode when a hole overflows contact -- a hole -- the gate electrode of MISFET and impurity diffusion field which are produced through the electric conduction object (an electric conduction plug or a part of wiring) with which it filled up inside -- simplistic -- the receiving margin can be enlarged

[0031]

[Embodiments of the Invention] Hereafter, with reference to a drawing, the gestalt of operation of this invention is explained in detail. In addition, in the complete diagram for explaining the gestalt of implementation of invention, what has the same function attaches the same sign, and explanation of the repeat is omitted.

[0032] (Operation gestalt 1) This operation gestalt explains the example which applied this invention to the semiconductor integrated circuit equipment which has two MOSFETs to the

element formation field of a semiconductor substrate.
[0033] Drawing 1 or drawing 10 is a cross section for explaining the manufacture method of the semiconductor integrated circuit equipment which is the operation gestalt 1 of this invention.
[0034] First, as shown in drawing 2 , a slot 2 is alternatively formed in the isolation field of the principal plane of the semiconductor substrate 1 which consists of single crystal silicon, after that, in a slot 2, the insulator layer 3 for isolation which consists of a silicon-oxide film is embedded, and between the element formation fields of the principal plane of the semiconductor substrate 1 is separated electrically.
[0035] Next, thermal oxidation processing is performed and the gate insulator layer 4 which consists of a silicon-oxide film of the thickness about 4 [nm] is formed on the element formation field of the semiconductor substrate 1.
[0036] Next, the polycrystal silicon film of the thickness for example, about [used as a gate electrode] 150 [nm] is formed by the CVD (Chemical VaporDeposition) method the whole surface on the semiconductor substrate 1 including the gate insulator layer 4 top. Phosphorus (P) is introduced into this polycrystal silicon film as an impurity which reduces resistance.
[0037] Next, the silicon-oxide film of the thickness for example, about [used as a cap insulator layer] 150 [nm] is formed by CVD the whole surface on the aforementioned polycrystal silicon film.
[0038] Next, the aforementioned silicon-oxide film and the aforementioned polycrystal silicon film are alike, respectively, anisotropic etching is given one by one, and the upper surface forms two gate electrodes 5 covered by the cap insulator layer 6 on the element formation field of the semiconductor substrate 1. Each of two gate electrodes 5 is formed where a predetermined interval is kept and arranged in parallel.
[0039] Next, the low concentration impurity diffusion field 7 which turns into a source field and a drain field by self-adjustment to the gate electrode 5 is formed in the element formation field of the semiconductor substrate 1. This low concentration impurity diffusion field 7 is formed by introducing arsenic (As) by the ion implantation method as an impurity. The process so far is shown in drawing 3 .
[0040] Next, the silicon oxide of the insulator layer 3 for isolation, the gate insulator layer 4, and cap insulator layer 6 grade and the semiconductor substrate 1, and the film that has selectivity to the silicon of gate electrode 5 grade (it is the film which can be etched alternatively), for example, a silicon nitride film, are formed by CVD the whole surface on the semiconductor substrate 1 including the cap insulator layer 6 top, and after that, anisotropic etching, such as RIE (Reactive Ion Etching), is given to the aforementioned silicon nitride film, and the sidewall spacer 8 is The sidewall spacer 8 is formed so that the width of face (thickness) of the direction of gate length may serve as for example, 100 [nm] grades. The process so far is shown in drawing 4 .
[0041] Next, the high concentration impurity diffusion field 9 which turns into a source field and a drain field by self-adjustment to the sidewall spacer 8 is formed in the element formation field of the semiconductor substrate 1. This high concentration impurity diffusion field 9 is formed by high impurity concentration higher than the low concentration impurity diffusion field 7. The high concentration impurity diffusion field 9 is formed by introducing arsenic (As) by the ion implantation method as an impurity. Of this process, n channel conductivity-type MOSFET-Q1 of the LDD structure where the portion by the side of the channel formation field of a drain field (low concentration impurity diffusion field 7) was set as low high impurity concentration

compared with the high impurity concentration of other portions (high concentration impurity diffusion field 9), and n channel conductivity-type MOSFET-Q2 of LDD structure are formed in the element formation field of the semiconductor substrate 1. Each of MOSFETQ1 and Q2 has the composition of mainly having the semiconductor substrate 1 used as a channel formation field, the gate insulator layer 4 which consists of a silicon-oxide film, the gate electrode 5 which consists of a polycrystal silicon film, the low concentration impurity diffusion field 7 of a couple used as a source field and a drain field, and the high concentration impurity diffusion field 9 of a couple used as a source field and a drain field. The upper surface is being worn by the cap insulator layer 6, and, as for the gate electrode 5, the side is being worn with the sidewall spacer 8. The low concentration impurity diffusion field 7 of a couple is formed by self-adjustment to the gate electrode 5, and the high concentration impurity diffusion field 9 of a couple is formed by self-adjustment to the sidewall spacer 8. Each gate electrode 5 of MOSFETQ1 and Q2 is arranged in parallel, and one high concentration diffusion field 9 of MOSFETQ1 is shared with one high concentration diffusion field 9 of MOSFETTQ2. The process so far is shown in drawing 5 .

[0042] Next, the sidewall spacer 8 is removed alternatively. The sidewall spacer 8 can be removed alternatively, without affecting the semiconductor substrate 1, the insulator layer 3 for isolation, the gate insulator layer 4, the gate electrode 5, and cap insulator layer 6 grade by carrying out, for example using the wet etching by the phosphoric acid, since the sidewall spacer 8 is formed by the silicon nitride film. The process so far is shown in drawing 6 .

[0043] Next, as the cap insulator layer 6 is covered, the etching stopper film 10 is formed by CVD the whole surface on the semiconductor substrate 1. The etching stopper film 10 is formed by the film which has selectivity to the silicon oxide of the insulator layer 3 for isolation, and cap insulator layer 6 grade, and the silicon of semiconductor substrate 1 grade (it is the film which can be etched alternatively), for example, a silicon nitride film. Moreover, the etching stopper film 10 is formed by thickness thicker than the thickness (width of face) of the direction of gate length of the sidewall spacer 8. The process so far is shown in drawing 7 .

[0044] Next, the layer insulation film 11 is formed on the etching stopper film 10. The layer insulation film 11 is formed with the film which has selectivity to the etching stopper film 10 (it is the film which can be etched alternatively), for example, a silicon-oxide film. The process so far is shown in drawing 8 .

[0045] next, each high concentration impurity diffusion field 9 top of MOSFETQ1 and Q2 -- the contact for diffusion fields -- the resist mask M1 for forming a hole is formed on the layer insulation film 11 using photolithography technology

[0046] Next, as the resist mask M1 is used as an etching mask and it is shown in drawing 9 Anisotropic etching is given to the layer insulation film 11 on the conditions which can take a selection ratio to the etching stopper film 10. Then, as anisotropic etching is given to the etching stopper film 10 on the conditions which can take a selection ratio to the semiconductor substrate 1, the insulator layer 3 for isolation, and cap insulator layer 6 grade which are the ground of the etching stopper film 10 and it is shown in drawing 10 the contact for diffusion fields which arrives at the high concentration impurity diffusion field 9 from the front face of the layer insulation film 11 -- a hole 12 is formed

[0047] Since the etching stopper film 10 is formed after removing alternatively the sidewall spacer 8 formed in the side of the gate electrode 5 in this process Anisotropic etching is given to each of the layer insulation film 11 and the etching stopper film 10. the high concentration

impurity diffusion field 9 top between the gate electrode 5 and the isolation field (insulator layer 3 for ** for elements) of the semiconductor substrate 1 -- the contact for diffusion fields -- in case a hole 12 is formed, the distance between the etching stopper films 10 and the isolation fields of the semiconductor substrate 1 which remain on the side of the gate electrode 5 becomes large The distance X between the gate electrode 5 and the isolation field of the semiconductor substrate 1 For example, 0.5 [mum], The width of face A of the direction of gate length of the sidewall spacer 8 0.1 [mum], the case where thickness B of the etching stopper film 10 is set to 0.1 [mum] -- the conventional technology -- the contact for diffusion fields -- the width of face which can carry out opening of the hole in order that the sidewall spacer 8 may place and replace the etching stopper film 10 with this operation form to becoming distance X-width-of-face A-thickness B= 0.3 [mum] -- the contact for diffusion fields -- the width of face which can carry out opening of the hole serves as distance X-thickness B= 0.4 [mum]

[0048] Moreover, since the etching stopper film 10 is formed after removing alternatively the sidewall spacer 8 formed in the side of the gate electrode 5 Anisotropic etching is given to each of the layer insulation film 11 and the etching stopper film 10. the high concentration impurity diffusion field 9 top between the gate electrodes 5 -- the contact for diffusion fields -- in case a hole 12 is formed, the distance between the etching stopper film 10 which remains on the side of one gate electrode 5, and the etching stopper film 10 which remains on the side of the gate electrode 5 of another side becomes large The width of face A of the direction of gate length of 0.6 [mum] and the sidewall spacer 8 for the distance Y between the gate electrodes 5 For example, 0.1 [mum], the case where thickness B of the etching stopper film 10 is set to 0.1 [mum] -- the conventional technology -- the contact for diffusion fields -- the width of face which can carry out opening of the hole distance Y-width-of-face Ax2-thickness Bx -- in order that the sidewall spacer 8 may place and replace the etching stopper film 10 with this operation form to being set to 2= 0.2 [mum] -- the contact for diffusion fields -- the width of face which can carry out opening of the hole -- distance Y-thickness Bx -- it is set to 2= 0.4 [mum]

[0049] next -- although the resist mask M1 is removed and not being illustrated after that -- the connection for diffusion fields -- the connection for the gates which reaches the gate electrode 5 from the front face of the layer insulation film 11 using the same method as a hole 12 -- a hole is formed

[0050] next, the connection for diffusion fields -- the inside of a hole 12, and the connection for the gates -- a hole -- by being filled up with electric conduction objects, such as a metal, inside, forming the electric conduction plug 14 in it, and forming wiring 15 on the layer insulation film 11 after that, as shown in drawing 1 , MOSFETQ1 and Q2 are alike, respectively, and the upper wiring 15 is connected electrically

[0051] According to this operation form, the following effects are acquired as explained above.

[0052] (1) By forming the etching stopper film 10, after removing alternatively the sidewall spacer 8 formed in the side of the gate electrode 5 Anisotropic etching is given to each of the layer insulation film 11 and the etching stopper film 10. the high concentration impurity diffusion field 9 top between the gate electrode 5 and the isolation field (insulator layer 3 for ** for elements) of the semiconductor substrate 1 -- the contact for diffusion fields, in case a hole 12 is formed the contact for diffusion fields in during this period since the distance between the etching stopper films 10 and the isolation fields of the semiconductor substrate 1 which remain on the side of the gate electrode 5 becomes large -- the area of base (exposed-surface product of the high concentration impurity diffusion field 9) of a hole 12 can be increased Consequently, the

contact resistance in the high concentration impurity diffusion field 9 of MOSFET (Q1, Q2) can be reduced.

[0053] moreover, the contact for diffusion fields between the etching stopper films 10 and the isolation fields of the semiconductor substrate 1 which remain on the side of the gate electrode 5 -- since the area of base (exposed-surface product of the high concentration impurity diffusion field 9) of a hole 12 can be increased -- this contact for diffusion fields -- detailed-ization of the part equivalent to the increase in the area of base of a hole 12 and MOSFET (Q1, Q2) can be attained

[0054] (2) By forming the etching stopper film 10, after removing alternatively the sidewall spacer 8 formed in the side of the gate electrode 5 Anisotropic etching is given to each of the layer insulation film 11 and the etching stopper film 10. the high concentration impurity diffusion field 9 top between the gate electrodes 5 -- the contact for diffusion fields, in case a hole 12 is formed Since the distance between the etching stopper film 10 which remains on the side of one gate electrode 5, and the etching stopper film 10 which remains on the side of the gate electrode 5 of another side becomes large the contact for diffusion fields in during this period -- the area of base (exposed-surface product of the high concentration impurity diffusion field 9) of a hole 12 can be increased Consequently, the contact resistance in the high concentration impurity diffusion field 9 of MOSFET (Q1, Q2) can be reduced.

[0055] moreover, the contact for diffusion fields between the etching stopper film 10 which remains on the side of one gate electrode 5, and the etching stopper film 10 which remains on the side of the gate electrode of another side -- since the area of base (exposed-surface product of the high concentration impurity diffusion field 9) of a hole 12 can be increased -- this contact for diffusion fields -- detailed-ization of the part equivalent to the increase in the area of base of a hole 12 and MOSFET (Q1, Q2) can be attained

[0056] (3) forming the etching stopper film 10 by thickness thicker than the width of face (thickness) of the direction of gate length of the sidewall spacer 8 -- the contact for diffusion fields -- since exposure of the low impurity diffusion field 7 can be prevented in case a hole 12 is formed, the increase in the leakage current in the shallow low impurity diffusion field 7 of junction can be suppressed

[0057] (4) making the amount of over etching of the etching stopper film 10 below into the thickness of the cap insulator layer 6 -- the contact for diffusion fields -- even if a hole 12 runs aground on the gate electrode 5, without it exposes the gate electrode 5 -- the contact for diffusion fields -- a hole 12 can be formed

[0058] In addition, although this operation form explained the example which formed the etching stopper film 10 by the silicon nitride film, since the etching stopper film 10 should just have selectivity to a ground, it is not limited to a silicon nitride film.

[0059] (Operation form 2) this operation form -- the element formation field top of a semiconductor substrate -- setting -- the connection for the gates -- the example which forms a hole is explained

[0060] Drawing 11 or drawing 17 is a cross section for explaining the manufacture method of the semiconductor integrated circuit equipment which is the operation form 2 of this invention.

[0061] First, a slot 2 is alternatively formed in the isolation field of the principal plane of the semiconductor substrate 1 which consists of single crystal silicon, after that, in a slot 2, the insulator layer 3 for isolation which consists of a silicon-oxide film is embedded, and between the element formation fields of the principal plane of the semiconductor substrate 1 is separated

electrically.
[0062] Next, using the same method as the above-mentioned operation form 1, as shown in drawing 12 , n channel type MOSFET-Q3 of LDD structure is formed in the element formation field of the semiconductor substrate 1. MOSFETQ3 has the composition of mainly having the semiconductor substrate 1 used as a channel formation field, the gate insulator layer 4 which consists of a silicon-oxide film, the gate electrode 5 which consists of a polycrystal silicon film, the low concentration impurity diffusion field 7 of a couple used as a source field and a drain field, and the high concentration impurity diffusion field 9 of a couple used as a source field and a drain field. The upper surface is being worn by the cap insulator layer 6, and, as for the gate electrode 5, the side is being worn with the sidewall spacer 8. The low concentration impurity diffusion field 7 of a couple is formed by self-adjustment to the gate electrode 5, and the high concentration impurity diffusion field 9 of a couple is formed by self-adjustment to the sidewall spacer 8.
[0063] Next, without affecting the semiconductor substrate 1, the insulator layer 3 for isolation, the gate insulator layer 4, the gate electrode 5, and cap insulator layer 6 grade, as shown in drawing 13 , the sidewall spacer 8 is removed alternatively.
[0064] Next, as the cap insulator layer 6 is covered, the etching stopper film 10 is formed by CVD the whole surface on the semiconductor substrate 1. The etching stopper film 10 is formed by the film which has selectivity to the silicon oxide of the insulator layer 3 for isolation, and cap insulator layer 6 grade, and the silicon of semiconductor substrate 1 grade (it is the film which can be etched alternatively), for example, a silicon nitride film. Moreover, the etching stopper film 10 is formed by thickness thicker than the width of face (thickness) of the direction of gate length of the sidewall spacer 8.
[0065] Next, as shown in drawing 14 , the layer insulation film 11 is formed on the etching stopper film 10. The layer insulation film 11 is formed with the film which has selectivity to the etching stopper film 10 (it is the film which can be etched alternatively), for example, a silicon-oxide film.
[0066] next, the contact for diffusion fields which arrives at the high concentration impurity diffusion field 9 from the front face of the layer insulation film 11 using the same method as the above-mentioned operation form 1 although not illustrated -- a hole is formed
[0067] next, the gate electrode 5 top -- the contact for the gates -- the resist mask M2 for forming a hole is formed on the layer insulation film 11 using photolithography technology
[0068] Next, as the resist mask M2 is used as an etching mask and it is shown in drawing 15 As anisotropic etching is given to the layer insulation film 11 on the conditions which can take a selection ratio to the etching stopper film 10 and it is shown in drawing 16 after that As anisotropic etching is given to the etching stopper film 10 on the conditions which can take a selection ratio to the cap insulator layer 6 and it is shown in drawing 17 after that the contact for the gates which gives anisotropic etching to the cap insulator layer 6 on the conditions which can take a selection ratio to the gate electrode 5 and the etching stopper film 10, and reaches the gate electrode 5 from the front face of the layer insulation film 11 -- a hole 13 is formed
[0069] since the etching stopper film 10 which has selectivity to the cap insulator layer 6 is formed after removing alternatively the sidewall spacer 8 formed in the side of the gate electrode 5 in this process -- the contact for the gates from the gate electrode 5 -- when a hole 13 overflows, the amount of over etching which can approve when **********ing the cap insulator layer 6 serves as a grade equivalent to the thickness which added the cap insulator layer 6 to the

thickness of the gate electrode 5 For example, when thickness of 150 [nm] and the cap insulator layer 6 is set to 150 [nm] for the thickness of the gate electrode 5, As opposed to the amount of over etching permissible with the conventional technology serving as 150 [nm] grades equivalent to the thickness of the gate electrode 5 a book -- operation -- a gestalt -- **** -- the gate -- an electrode -- five -- the side -- a cap -- an insulator layer -- six -- receiving -- selectivity -- having -- etching -- a stopper -- a film -- ten -- covering -- having -- **** -- a sake -- being permissible -- over etching -- an amount -- the gate -- an electrode -- five -- thickness -- a cap -- an insulator layer -- six -- thickness -- having added -- thickness -- corresponding -- 300 -- [-- nm --] -- a grade --

[0070] next, the resist mask M2 -- removing -- the connection for after that and diffusion fields -- a hole -- inside and the connection for the gates -- by being filled up with electric conduction objects, such as a metal, forming the electric conduction plug 14 in a hole 13, and forming wiring 15 on the layer insulation film 11 after that, as shown in drawing 11 , the upper wiring 15 is electrically connected to MOSFETQ3

[0071] According to this operation gestalt, the following effects are acquired as explained above.

[0072] By forming the etching stopper film 10 which has selectivity to the cap insulator layer 6, after removing alternatively the sidewall spacer 8 formed in the side of the gate electrode 5 the contact for the gates from the gate electrode 5, when a hole 13 overflows Since the amount of over etching which can approve when **********ing the cap insulator layer 6 serves as a grade equivalent to the thickness which added the cap insulator layer 6 to the thickness of the gate electrode 5 the contact for the gates -- the gate electrode 5 of MOSFETQ3 and impurity diffusion field (7 9) which are produced through the electric conduction object (the electric conduction plug 14 or a part of wiring) with which it filled up in the hole 13 -- simplistic -- the receiving margin can be enlarged

[0073] moreover, the gate electrode 5 of MOSFETQ3 and an impurity diffusion field (7 9) -- simplistic -- since the receiving margin can be enlarged -- the element formation field top of the semiconductor substrate 1 -- setting -- the contact for the gates -- a hole 13 can be formed easily and detailed-ization of MOSFETQ3 can be attained

[0074] In addition, although this operation gestalt explained the example which formed the etching stopper film 10 by the silicon nitride film, since the etching stopper film 10 should just have selectivity to a cap insulator layer and a gate electrode at least, it is not limited to a silicon nitride film.

[0075] Moreover, although the operation gestalt 1 and the operation gestalt 2 explained the example using MOSFET of the LDD structure which formed the low concentration impurity diffusion field by the ion implantation method, you may be MOSFET of the LDD structure which formed the sidewall spacer with which the impurity was introduced into the side of a gate electrode, diffused the impurity from this sidewall spacer and formed the low concentration impurity diffusion field.

[0076] Moreover, although the operation gestalt 1 and the operation gestalt 2 explained the example which used the n channel conductivity type MOSFET, you may be the p-channel conductivity type MOSFET.

[0077] Moreover, although the operation gestalt 1 and the operation gestalt 2 explained the example which used MOSFET, it is not limited to this but the thing which may be MISFET is undoubted. The gate insulator layer of MISFET is formed by the Si-O-N film which oxidized for example, the thermal oxidation film in N2O gas atmosphere. For example, hot carrier resistance

of MISFET using the gate insulator layer which consists of this Si-O-N film improves.
[0078] As mentioned above, although invention made by this invention person was concretely explained based on the aforementioned operation gestalt, this invention of the ability to change variously in the range which is not limited to the aforementioned operation gestalt and does not deviate from the summary is natural.
[0079]
[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated in this application is explained briefly.
[0080] It becomes possible to reduce the contact resistance in the impurity diffusion field of MISFET.
[0081] Moreover, it becomes possible to enlarge the margin to the short circuit of the gate electrode of MISFET, and an impurity diffusion field.
[0082] Moreover, it becomes possible to attain detailed-ization of MISFET.

[Translation done.]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD [The technical field to which invention belongs] Especially this invention is applied to the semiconductor integrated circuit equipment which has MISFET (Metal Insulator Semiconductor Field Effect Transistor) of LDD (Lightly Doped Drain) structure about semiconductor integrated circuit equipment, and relates to effective technology.

[Translation done.]

* NOTICES *

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PRIOR ART [Description of the Prior Art] MOSFET (Metal Oxide Semiconductor Field Effect Transistor) accumulated by semiconductor integrated circuit equipment turns minutely with high integration, and adoption of the LDD structure where the portion by the side of the channel formation field of a drain field was set as low high impurity concentration compared with the high impurity concentration of other portions serves as indispensable requirements in MOSFET to which a gate-length size reaches submicron one especially. Since MOSFET of this LDD structure reduces the amount of diffusion by the side of the channel formation field of a drain field and can secure a channel-length size, it can suppress generating of a short channel effect. Moreover, MOSFET of LDD structure eases the inclination of the impurity atom concentration profile of the pn junction section formed between a drain field and a channel formation field, and since it can weaken the field strength generated to this field, it can suppress generating of the hot carrier effect.
[0003] by the way -- in order to attain high integration of semiconductor integrated circuit equipment -- detailed-izing, simultaneously " of a processing size -- a gate electrode and contact -- the doubling between each structure distance" between holes needs to be reduced an impurity diffusion field [which turns into a source field of MOSFET, and a drain field now using SAC (Self Aligned Contact hole) technology], and gate electrode top -- self-adjustment -- contact -- contact of as opposed to [form a hole and] the gate electrode of the isolation field of a semiconductor substrate or MOSFET -- reduction of the doubling margin of a hole is aimed at
[0004] About SAC technology, they are eye I dee em 93[IEDM93, and p441 and A, for example. It is indicated by Novel Borderless Contact/Interconnect Technology Using Aluminum Oxide Etch Stop for High Performance SRAM and Logic].

[Translation done.]

* NOTICES *

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EFFECT OF THE INVENTION [Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated in this application is explained briefly.
[0080] It becomes possible to reduce the contact resistance in the impurity diffusion field of MISFET.
[0081] Moreover, it becomes possible to enlarge the margin to the short circuit of the gate electrode of MISFET, and an impurity diffusion field.
[0082] Moreover, it becomes possible to attain detailed-ization of MISFET.

[Translation done.]

* NOTICES *

TECHNICAL PROBLEM [Problem(s) to be Solved by the Invention] the SAC technology after forming MOSFET of LDD structure -- using -- contact -- the trouble in the case of forming a hole is explained using drawing 18 or drawing 22 (cross section for explaining the manufacture method)

[0006] First, a slot 22 is formed in the isolation field of the principal plane of a silicon substrate 21, after that, in a slot 22, the insulator layer 23 for isolation which consists of a silicon-oxide film is embedded, and between the element formation fields of the principal plane of a silicon substrate 21 is separated electrically.

[0007] Next, as shown in drawing 18 , MOSFET-Q4 of LDD structure and MOSFET-Q5 of LDD structure are formed in the element formation field of a silicon substrate 21. Each of MOSFETQ4 and Q5 has the composition of mainly having the silicon substrate 21 used as a channel formation field, the gate insulator layer 24 which consists of a silicon-oxide film, the gate electrode 25 which consists of a polycrystal silicon film, the low concentration impurity diffusion field 27 of a couple used as a source field and a drain field, and the high concentration impurity diffusion field 29 of a couple used as a source field and a drain field. The gate electrode 25 is covered by the cap insulator layer 26 which the upper surface becomes from a silicon-oxide film, and is covered with the sidewall spacer (side-attachment-wall insulator layer) 28 with which the side (side attachment wall) consists of a silicon-oxide film. The low concentration impurity diffusion field 27 of a couple is formed by self-adjustment to the gate electrode 25, and the high concentration impurity diffusion field 29 of a couple is formed by self-adjustment to the sidewall spacer 28. Each gate electrode 25 of MOSFETQ4 and Q5 is arranged in parallel. One high concentration impurity diffusion field 29 of MOSFETQ4 is shared with one high concentration impurity diffusion field 29 of MOSFETQ5.

[0008] Next, as are shown in drawing 19 , and the cap insulator layer 26 and the sidewall spacer 28 are covered, the etching stopper film 30 is formed the whole surface on a silicon substrate 21. The etching stopper film 30 is formed by the film which has selectivity to the silicon oxide of the insulator layer 23 for isolation, the cap insulator layer 26, and sidewall spacer 28 grade, and the silicon of silicon-substrate 21 grade (it is the film which can be etched alternatively), for example, a silicon nitride film.

[0009] Next, the layer insulation film 31 is formed on the etching stopper film 30. The layer insulation film 31 forms the film (it is the film which can be etched alternatively) and metaphor of having selectivity to the etching stopper film 30, by the silicon-oxide film.

[0010] next, each high concentration impurity diffusion field 29 top of MOSFETQ4 and Q5 -- the contact for diffusion fields -- the resist mask M3 for forming a hole is formed on the layer insulation film 31 using photolithography technology

[0011] Next, as the resist mask M3 is used as an etching mask and it is shown in drawing 20 Anisotropic etching is given to the layer insulation film 31 on the conditions which can take a selection ratio to the etching stopper film 30. Then, anisotropic etching is given to the etching stopper film 30 on the conditions which can take a selection ratio to the silicon oxide of the insulator layer 23 for isolation which is the ground of the etching stopper film 30, the cap insulator layer 26, and sidewall spacer 28 grade, and the silicon of silicon-substrate 21 grade. the contact for diffusion fields which arrives at the high concentration impurity diffusion field 29 from the front face of the layer insulation film 31 as shown in drawing 21 -- a hole 32 is formed
[0012] next -- although the resist mask M3 is removed and not being illustrated after that -- the contact for diffusion fields -- the contact for the gates which reaches the gate electrode 25 from the front face of the layer insulation film 31 using the same method as a hole 32 -- a hole is formed
[0013] next, the contact for diffusion fields -- the inside of a hole 32, and the contact for the gates -- a hole -- by being filled up with electric conduction objects, such as a metal, inside, forming the electric conduction plug 14 in it, and forming wiring 15 in it after that, as shown in drawing 22 , MOSFETQ4 and Q5 are alike, respectively, and the upper wiring 15 is connected electrically
[0014] the ** which will not affect the sidewall spacer 28 and the insulator layer 23 for isolation if the above-mentioned method is used -- the contact for diffusion fields -- since a hole 32 can be formed -- the gate electrode 25 and the contact for diffusion fields -- the distance between holes 32 is reducible
[0015] however, since thickness looks thick in efficiency as anisotropic etching like the sidewall spacer 28 when the etching stopper film 30 is formed in a perpendicular portion to a silicon substrate 31, it is shown in drawing 21 -- as -- the contact for diffusion fields -- the etching stopper film 30 remains thickly in the shape of a side attachment wall by side of the sidewall spacer 28 by the anisotropic etching when forming a hole 32 for this reason, the contact for diffusion fields -- the low area (exposed-surface product of a high concentration impurity diffusion field) of a hole 32 contracts, and there is a problem that the contact resistance in the high concentration impurity diffusion field 29 between the isolation field (insulator layer 23 for isolation) of a silicon substrate 21 and the gate electrode 25 and the contact resistance in the high concentration impurity diffusion field 29 between the gate electrodes 25 increase
[0016] moreover, the element formation field top of a silicon substrate -- setting -- the contact for the gates -- the trouble in the case of forming a hole is explained using drawing 23 (cross section for explaining the manufacture method)
[0017] the gate electrode 25 top of MOSFET-Q6 -- the contact for the gates -- the resist mask M4 for forming a hole is formed on the layer insulation film 31 using photolithography technology
[0018] Next, use the resist mask M4 as an etching mask, and anisotropic etching is given to the layer insulation film 31 on the conditions which can take selectivity to the etching stopper film 30. Then, anisotropic etching is given to the etching stopper film 30 on the conditions which can take a selection ratio to the cap insulator layer 26 and the sidewall spacer 28. then, the contact for the gates which reaches from the upper surface of the layer insulation film 31 on the element formation field of a silicon substrate 21 at the gate electrode 25 by giving anisotropic etching to the cap insulator layer 26 on the conditions which can take a selection ratio to the gate electrode 25 -- a hole 33 can be formed
[0019] making the amount of over etching at the time of etching of the cap insulator layer 26 below into the thickness of the gate electrode 25, if the above-mentioned method is used -- the

contact for the gates from the gate electrode 25 -- even if it is a case so that a hole 33 may overflow, without it exposes the low concentration impurity diffusion field 27 and the high concentration impurity diffusion field 29 -- the contact for the gates -- a hole 33 can be formed
[0020] however -- since the permissible amount of over etching has only a grade equivalent to the thickness of the gate electrode 25 -- the contact for the gates -- the gate electrode and impurity diffusion field which are produced through the electric conduction object (an electric conduction plug or a part of wiring) with which it filled up in the hole 33 -- simplistic -- the receiving margin is small
[0021] The purpose of this invention is to offer the technology which can reduce the contact resistance in the impurity diffusion field of MISFET.
[0022] other purposes of this invention -- the gate electrode of MISFET, and an impurity diffusion field -- simplistic -- it is in offering the technology which can enlarge the receiving margin
[0023] The other purposes and the new feature will become clear by description and the accompanying drawing of this specification at the aforementioned row of this invention.

[Translation done.]

MEANS [Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0025] It has MISFET to the element formation field of a semiconductor substrate. (1) Above MISFET The gate electrode by which the upper surface was being worn by the cap insulator layer, and the side was being worn with the sidewall spacer, The low concentration impurity diffusion field formed by self-adjustment to the aforementioned gate electrode, It is the manufacture method of the semiconductor integrated circuit equipment which has the composition of having the high concentration impurity diffusion field formed by self-adjustment to the aforementioned sidewall spacer. Remove the aforementioned sidewall spacer alternatively and the etching stopper film which has selectivity to a ground on the aforementioned semiconductor substrate as covers the aforementioned cap insulator layer is formed after that. Then, the process which forms the layer insulation film which has selectivity to it on the aforementioned etching stopper film, Give anisotropic etching on the conditions which can take a selection ratio to the aforementioned etching stopper film on the aforementioned layer insulation film, and anisotropic etching is given after that on the conditions which can take a selection ratio to the ground on the aforementioned etching stopper film. the contact which arrives at the aforementioned high concentration impurity diffusion field from the front face of the aforementioned layer insulation film -- it has the process which forms a hole
[0026] It has each of the first MISFET and the second MISFET to the element formation field of a semiconductor substrate. (2) Each of the first above MISFET and the second MISFET The gate electrode by which the upper surface was being worn by the cap insulator layer, and the side was being worn with the sidewall spacer, The low concentration impurity diffusion field of the couple formed by self-adjustment to the aforementioned gate electrode, It has the composition of having the high concentration impurity diffusion field of the couple formed by self-adjustment to the aforementioned sidewall spacer. The first above MISFET and each gate electrode of the second MISFET are arranged in parallel. one high concentration impurity diffusion field of the first above MISFET It is the manufacture method of the semiconductor integrated circuit equipment currently shared with one high concentration impurity diffusion field of the second above MISFET in the aforementioned gate inter-electrode. Remove the aforementioned sidewall spacer alternatively and the etching stopper film which has selectivity to a ground on the aforementioned semiconductor substrate as covers the aforementioned cap insulator layer is formed after that. Then, the process which forms the layer insulation film which has selectivity to it on the aforementioned etching stopper film, Give anisotropic etching on the conditions which can take a selection ratio to the aforementioned etching stopper film on the aforementioned layer insulation film, and anisotropic etching is given after that on the conditions which can take a

selection ratio to the ground on the aforementioned etching stopper film. the contact which arrives at the aforementioned high concentration impurity diffusion field from the front face of the aforementioned layer insulation film -- it has the process which forms a hole

[0027] It has MISFET to the element formation field of a semiconductor substrate. (3) Above MISFET The gate electrode by which the upper surface was being worn by the cap insulator layer, and the side was being worn with the sidewall spacer, The low concentration impurity diffusion field formed by self-adjustment to the aforementioned gate electrode, It is the manufacture method of the semiconductor integrated circuit equipment which has the composition of having the high concentration impurity diffusion field formed by self-adjustment to the aforementioned sidewall spacer. Remove the aforementioned sidewall spacer alternatively and the etching stopper film which has selectivity to a ground on the aforementioned semiconductor substrate as covers the aforementioned cap insulator layer is formed after that. Then, the process which forms the layer insulation film which has selectivity to it on the aforementioned etching stopper film, Anisotropic etching is given on the conditions which can take a selection ratio to the aforementioned etching stopper film on the aforementioned layer insulation film. Then, anisotropic etching is given on the conditions which can take a selection ratio to the ground on the aforementioned etching stopper film. then, the contact which gives anisotropic etching on the conditions which can take a selection ratio to the aforementioned gate electrode and the aforementioned etching stopper film to the aforementioned cap insulator layer, and reaches the aforementioned gate electrode from the front face of the aforementioned layer insulation film -- it has the process which forms a hole

[0028] By forming an etching stopper film, after removing alternatively the sidewall spacer formed in the side of a gate electrode according to the means (1) mentioned above Anisotropic etching is given to each of a layer insulation film and an etching stopper film. the high concentration impurity diffusion field top between a gate electrode and the isolation field of a semiconductor substrate -- contact, since the distance between the etching stopper films and the isolation fields of a semiconductor substrate which remain on the side of a gate electrode becomes large in case a hole is formed the contact in during this period -- the area of base (exposed-surface product of a high concentration impurity diffusion field) of a hole can be increased Consequently, the contact resistance in the high concentration impurity diffusion field of MISFET can be reduced.

[0029] By forming an etching stopper film, after removing alternatively the sidewall spacer formed in the side of a gate electrode according to the means (2) mentioned above Anisotropic etching is given to each of a layer insulation film and an etching stopper film. a gate inter-electrode high concentration impurity diffusion field top -- contact, since the distance between the etching stopper film which remains on the side of one gate electrode, and the etching stopper film which remains on the side of the gate electrode of another side becomes large in case a hole is formed the contact in during this period -- the area of base (exposed-surface product of a high concentration impurity diffusion field) of a hole can be increased Consequently, the contact resistance in the high concentration impurity diffusion field of MISFET can be reduced.

[0030] By forming the etching stopper film which has selectivity to a cap insulator layer, after removing alternatively the sidewall spacer formed in the side of a gate electrode according to the means (3) mentioned above the contact from a gate electrode, since the amount of over etching which can approve when **********ing a cap insulator layer serves as a grade equivalent to the

thickness which added the cap insulator layer to the thickness of a gate electrode when a hole overflows contact -- a hole -- the gate electrode of MISFET and impurity diffusion field which are produced through the electric conduction object (an electric conduction plug or a part of wiring) with which it filled up inside -- simplistic -- the receiving margin can be enlarged
[0031]
[Embodiments of the Invention] Hereafter, with reference to a drawing, the form of operation of this invention is explained in detail. In addition, in the complete diagram for explaining the form of implementation of invention, what has the same function attaches the same sign, and explanation of the repeat is omitted.
[0032] (Operation form 1) This operation form explains the example which applied this invention to the semiconductor integrated circuit equipment which has two MOSFETs to the element formation field of a semiconductor substrate.
[0033] Drawing 1 or drawing 10 is a cross section for explaining the manufacture method of the semiconductor integrated circuit equipment which is the operation form 1 of this invention.
[0034] First, as shown in drawing 2 , a slot 2 is alternatively formed in the isolation field of the principal plane of the semiconductor substrate 1 which consists of single crystal silicon, after that, in a slot 2, the insulator layer 3 for isolation which consists of a silicon-oxide film is embedded, and between the element formation fields of the principal plane of the semiconductor substrate 1 is separated electrically.
[0035] Next, thermal oxidation processing is performed and the gate insulator layer 4 which consists of a silicon-oxide film of the thickness about 4 [nm] is formed on the element formation field of the semiconductor substrate 1.
[0036] Next, the polycrystal silicon film of the thickness for example, about [used as a gate electrode] 150 [nm] is formed by the CVD (Chemical VaporDeposition) method the whole surface on the semiconductor substrate 1 including the gate insulator layer 4 top. Phosphorus (P) is introduced into this polycrystal silicon film as an impurity which reduces resistance.
[0037] Next, the silicon-oxide film of the thickness for example, about [used as a cap insulator layer] 150 [nm] is formed by CVD the whole surface on the aforementioned polycrystal silicon film.
[0038] Next, the aforementioned silicon-oxide film and the aforementioned polycrystal silicon film are alike, respectively, anisotropic etching is given one by one, and the upper surface forms two gate electrodes 5 covered by the cap insulator layer 6 on the element formation field of the semiconductor substrate 1. Each of two gate electrodes 5 is formed where a predetermined interval is kept and arranged in parallel.
[0039] Next, the low concentration impurity diffusion field 7 which turns into a source field and a drain field by self-adjustment to the gate electrode 5 is formed in the element formation field of the semiconductor substrate 1. This low concentration impurity diffusion field 7 is formed by introducing arsenic (As) by the ion implantation method as an impurity. The process so far is shown in drawing 3 .
[0040] Next, the silicon oxide of the insulator layer 3 for isolation, the gate insulator layer 4, and cap insulator layer 6 grade and the semiconductor substrate 1, and the film that has selectivity to the silicon of gate electrode 5 grade (it is the film which can be etched alternatively), for example, a silicon nitride film, are formed by CVD the whole surface on the semiconductor substrate 1 including the cap insulator layer 6 top, and after that, anisotropic etching, such as RIE (Reactive Ion Etching), is given to the aforementioned silicon nitride film, and the sidewall

spacer 8 is The sidewall spacer 8 is formed so that the width of face (thickness) of the direction of gate length may serve as for example, 100 [nm] grades. The process so far is shown in drawing 4 .

[0041] Next, the high concentration impurity diffusion field 9 which turns into a source field and a drain field by self-adjustment to the sidewall spacer 8 is formed in the element formation field of the semiconductor substrate 1. This high concentration impurity diffusion field 9 is formed by high impurity concentration higher than the low concentration impurity diffusion field 7. The high concentration impurity diffusion field 9 is formed by introducing arsenic (As) by the ion implantation method as an impurity. Of this process, n channel conductivity-type MOSFET-Q1 of the LDD structure where the portion by the side of the channel formation field of a drain field (low concentration impurity diffusion field 7) was set as low high impurity concentration compared with the high impurity concentration of other portions (high concentration impurity diffusion field 9), and n channel conductivity-type MOSFET-Q2 of LDD structure are formed in the element formation field of the semiconductor substrate 1. Each of MOSFETQ1 and Q2 has the composition of mainly having the semiconductor substrate 1 used as a channel formation field, the gate insulator layer 4 which consists of a silicon-oxide film, the gate electrode 5 which consists of a polycrystal silicon film, the low concentration impurity diffusion field 7 of a couple used as a source field and a drain field, and the high concentration impurity diffusion field 9 of a couple used as a source field and a drain field. The upper surface is being worn by the cap insulator layer 6, and, as for the gate electrode 5, the side is being worn with the sidewall spacer 8. The low concentration impurity diffusion field 7 of a couple is formed by self-adjustment to the gate electrode 5, and the high concentration impurity diffusion field 9 of a couple is formed by self-adjustment to the sidewall spacer 8. Each gate electrode 5 of MOSFETQ1 and Q2 is arranged in parallel, and one high concentration diffusion field 9 of MOSFETQ1 is shared with one high concentration diffusion field 9 of MOSFETTQ2. The process so far is shown in drawing 5 .

[0042] Next, the sidewall spacer 8 is removed alternatively. The sidewall spacer 8 can be removed alternatively, without affecting the semiconductor substrate 1, the insulator layer 3 for isolation, the gate insulator layer 4, the gate electrode 5, and cap insulator layer 6 grade by carrying out, for example using the wet etching by the phosphoric acid, since the sidewall spacer 8 is formed by the silicon nitride film. The process so far is shown in drawing 6 .

[0043] Next, as the cap insulator layer 6 is covered, the etching stopper film 10 is formed by CVD the whole surface on the semiconductor substrate 1. The etching stopper film 10 is formed by the film which has selectivity to the silicon oxide of the insulator layer 3 for isolation, and cap insulator layer 6 grade, and the silicon of semiconductor substrate 1 grade (it is the film which can be etched alternatively), for example, a silicon nitride film. Moreover, the etching stopper film 10 is formed by thickness thicker than the thickness (width of face) of the direction of gate length of the sidewall spacer 8. The process so far is shown in drawing 7 .

[0044] Next, the layer insulation film 11 is formed on the etching stopper film 10. The layer insulation film 11 is formed with the film which has selectivity to the etching stopper film 10 (it is the film which can be etched alternatively), for example, a silicon-oxide film. The process so far is shown in drawing 8 .

[0045] next, each high concentration impurity diffusion field 9 top of MOSFETQ1 and Q2 -- the contact for diffusion fields -- the resist mask M1 for forming a hole is formed on the layer insulation film 11 using photolithography technology

[0046] Next, as the resist mask M1 is used as an etching mask and it is shown in drawing 9 Anisotropic etching is given to the layer insulation film 11 on the conditions which can take a selection ratio to the etching stopper film 10. Then, as anisotropic etching is given to the etching stopper film 10 on the conditions which can take a selection ratio to the semiconductor substrate 1, the insulator layer 3 for isolation, and cap insulator layer 6 grade which are the ground of the etching stopper film 10 and it is shown in drawing 10 the contact for diffusion fields which arrives at the high concentration impurity diffusion field 9 from the front face of the layer insulation film 11 -- a hole 12 is formed

[0047] Since the etching stopper film 10 is formed after removing alternatively the sidewall spacer 8 formed in the side of the gate electrode 5 in this process Anisotropic etching is given to each of the layer insulation film 11 and the etching stopper film 10. the high concentration impurity diffusion field 9 top between the gate electrode 5 and the isolation field (insulator layer 3 for ** for elements) of the semiconductor substrate 1 -- the contact for diffusion fields -- in case a hole 12 is formed, the distance between the etching stopper films 10 and the isolation fields of the semiconductor substrate 1 which remain on the side of the gate electrode 5 becomes large The distance X between the gate electrode 5 and the isolation field of the semiconductor substrate 1 For example, 0.5 [mum], The width of face A of the direction of gate length of the sidewall spacer 8 0.1 [mum], the case where thickness B of the etching stopper film 10 is set to 0.1 [mum] -- the conventional technology -- the contact for diffusion fields -- the width of face which can carry out opening of the hole in order that the sidewall spacer 8 may place and replace the etching stopper film 10 with this operation gestalt to becoming distance X-width-of-face A-thickness B= 0.3 [mum] -- the contact for diffusion fields -- the width of face which can carry out opening of the hole serves as distance X-thickness B= 0.4 [mum]

[0048] Moreover, since the etching stopper film 10 is formed after removing alternatively the sidewall spacer 8 formed in the side of the gate electrode 5 Anisotropic etching is given to each of the layer insulation film 11 and the etching stopper film 10. the high concentration impurity diffusion field 9 top between the gate electrodes 5 -- the contact for diffusion fields -- in case a hole 12 is formed, the distance between the etching stopper film 10 which remains on the side of one gate electrode 5, and the etching stopper film 10 which remains on the side of the gate electrode 5 of another side becomes large The width of face A of the direction of gate length of 0.6 [mum] and the sidewall spacer 8 for the distance Y between the gate electrodes 5 For example, 0.1 [mum], the case where thickness B of the etching stopper film 10 is set to 0.1 [mum] -- the conventional technology -- the contact for diffusion fields -- the width of face which can carry out opening of the hole distance Y-width-of-face Ax2-thickness Bx -- in order that the sidewall spacer 8 may place and replace the etching stopper film 10 with this operation gestalt to being set to 2= 0.2 [mum] -- the contact for diffusion fields -- the width of face which can carry out opening of the hole -- distance Y-thickness Bx -- it is set to 2= 0.4 [mum]

[0049] next -- although the resist mask M1 is removed and not being illustrated after that -- the connection for diffusion fields -- the connection for the gates which reaches the gate electrode 5 from the front face of the layer insulation film 11 using the same method as a hole 12 -- a hole is formed

[0050] next, the connection for diffusion fields -- the inside of a hole 12, and the connection for the gates -- a hole -- by being filled up with electric conduction objects, such as a metal, inside, forming the electric conduction plug 14 in it, and forming wiring 15 on the layer insulation film 11 after that, as shown in drawing 1 , MOSFETQ1 and Q2 are alike, respectively, and the upper

wiring 15 is connected electrically
[0051] According to this operation gestalt, the following effects are acquired as explained above.
[0052] (1) By forming the etching stopper film 10, after removing alternatively the sidewall spacer 8 formed in the side of the gate electrode 5 Anisotropic etching is given to each of the layer insulation film 11 and the etching stopper film 10. the high concentration impurity diffusion field 9 top between the gate electrode 5 and the isolation field (insulator layer 3 for ** for elements) of the semiconductor substrate 1 -- the contact for diffusion fields, in case a hole 12 is formed the contact for diffusion fields in during this period since the distance between the etching stopper films 10 and the isolation fields of the semiconductor substrate 1 which remain on the side of the gate electrode 5 becomes large -- the area of base (exposed-surface product of the high concentration impurity diffusion field 9) of a hole 12 can be increased Consequently, the contact resistance in the high concentration impurity diffusion field 9 of MOSFET (Q1, Q2) can be reduced.
[0053] moreover, the contact for diffusion fields between the etching stopper films 10 and the isolation fields of the semiconductor substrate 1 which remain on the side of the gate electrode 5 -- since the area of base (exposed-surface product of the high concentration impurity diffusion field 9) of a hole 12 can be increased -- this contact for diffusion fields -- detailed-ization of the part equivalent to the increase in the area of base of a hole 12 and MOSFET (Q1, Q2) can be attained
[0054] (2) By forming the etching stopper film 10, after removing alternatively the sidewall spacer 8 formed in the side of the gate electrode 5 Anisotropic etching is given to each of the layer insulation film 11 and the etching stopper film 10. the high concentration impurity diffusion field 9 top between the gate electrodes 5 -- the contact for diffusion fields, in case a hole 12 is formed Since the distance between the etching stopper film 10 which remains on the side of one gate electrode 5, and the etching stopper film 10 which remains on the side of the gate electrode 5 of another side becomes large the contact for diffusion fields in during this period -- the area of base (exposed-surface product of the high concentration impurity diffusion field 9) of a hole 12 can be increased Consequently, the contact resistance in the high concentration impurity diffusion field 9 of MOSFET (Q1, Q2) can be reduced.
[0055] moreover, the contact for diffusion fields between the etching stopper film 10 which remains on the side of one gate electrode 5, and the etching stopper film 10 which remains on the side of the gate electrode of another side -- since the area of base (exposed-surface product of the high concentration impurity diffusion field 9) of a hole 12 can be increased -- this contact for diffusion fields -- detailed-ization of the part equivalent to the increase in the area of base of a hole 12 and MOSFET (Q1, Q2) can be attained
[0056] (3) forming the etching stopper film 10 by thickness thicker than the width of face (thickness) of the direction of gate length of the sidewall spacer 8 -- the contact for diffusion fields -- since exposure of the low impurity diffusion field 7 can be prevented in case a hole 12 is formed, the increase in the leakage current in the shallow low impurity diffusion field 7 of junction can be suppressed
[0057] (4) making the amount of over etching of the etching stopper film 10 below into the thickness of the cap insulator layer 6 -- the contact for diffusion fields -- even if a hole 12 runs aground on the gate electrode 5, without it exposes the gate electrode 5 -- the contact for diffusion fields -- a hole 12 can be formed
[0058] In addition, although this operation gestalt explained the example which formed the

etching stopper film 10 by the silicon nitride film, since the etching stopper film 10 should just have selectivity to a ground, it is not limited to a silicon nitride film.
[0059] (Operation gestalt 2) this operation gestalt -- the element formation field top of a semiconductor substrate -- setting -- the connection for the gates -- the example which forms a hole is explained
[0060] Drawing 11 or drawing 17 is a cross section for explaining the manufacture method of the semiconductor integrated circuit equipment which is the operation gestalt 2 of this invention.
[0061] First, a slot 2 is alternatively formed in the isolation field of the principal plane of the semiconductor substrate 1 which consists of single crystal silicon, after that, in a slot 2, the insulator layer 3 for isolation which consists of a silicon-oxide film is embedded, and between the element formation fields of the principal plane of the semiconductor substrate 1 is separated electrically.
[0062] Next, using the same method as the above-mentioned operation gestalt 1, as shown in drawing 12 , n channel type MOSFET-Q3 of LDD structure is formed in the element formation field of the semiconductor substrate 1. MOSFETQ3 has the composition of mainly having the semiconductor substrate 1 used as a channel formation field, the gate insulator layer 4 which consists of a silicon-oxide film, the gate electrode 5 which consists of a polycrystal silicon film, the low concentration impurity diffusion field 7 of a couple used as a source field and a drain field, and the high concentration impurity diffusion field 9 of a couple used as a source field and a drain field. The upper surface is being worn by the cap insulator layer 6, and, as for the gate electrode 5, the side is being worn with the sidewall spacer 8. The low concentration impurity diffusion field 7 of a couple is formed by self-adjustment to the gate electrode 5, and the high concentration impurity diffusion field 9 of a couple is formed by self-adjustment to the sidewall spacer 8.
[0063] Next, without affecting the semiconductor substrate 1, the insulator layer 3 for isolation, the gate insulator layer 4, the gate electrode 5, and cap insulator layer 6 grade, as shown in drawing 13 , the sidewall spacer 8 is removed alternatively.
[0064] Next, as the cap insulator layer 6 is covered, the etching stopper film 10 is formed by CVD the whole surface on the semiconductor substrate 1. The etching stopper film 10 is formed by the film which has selectivity to the silicon oxide of the insulator layer 3 for isolation, and cap insulator layer 6 grade, and the silicon of semiconductor substrate 1 grade (it is the film which can be etched alternatively), for example, a silicon nitride film. Moreover, the etching stopper film 10 is formed by thickness thicker than the width of face (thickness) of the direction of gate length of the sidewall spacer 8.
[0065] Next, as shown in drawing 14 , the layer insulation film 11 is formed on the etching stopper film 10. The layer insulation film 11 is formed with the film which has selectivity to the etching stopper film 10 (it is the film which can be etched alternatively), for example, a silicon-oxide film.
[0066] next, the contact for diffusion fields which arrives at the high concentration impurity diffusion field 9 from the front face of the layer insulation film 11 using the same method as the above-mentioned operation gestalt 1 although not illustrated -- a hole is formed
[0067] next, the gate electrode 5 top -- the contact for the gates -- the resist mask M2 for forming a hole is formed on the layer insulation film 11 using photolithography technology
[0068] Next, as the resist mask M2 is used as an etching mask and it is shown in drawing 15 As anisotropic etching is given to the layer insulation film 11 on the conditions which can take a

selection ratio to the etching stopper film 10 and it is shown in drawing 16 after that As anisotropic etching is given to the etching stopper film 10 on the conditions which can take a selection ratio to the cap insulator layer 6 and it is shown in drawing 17 after that the contact for the gates which gives anisotropic etching to the cap insulator layer 6 on the conditions which can take a selection ratio to the gate electrode 5 and the etching stopper film 10, and reaches the gate electrode 5 from the front face of the layer insulation film 11 -- a hole 13 is formed

[0069] since the etching stopper film 10 which has selectivity to the cap insulator layer 6 is formed after removing alternatively the sidewall spacer 8 formed in the side of the gate electrode 5 in this process -- the contact for the gates from the gate electrode 5 -- when a hole 13 overflows, the amount of over etching which can approve when **********ing the cap insulator layer 6 serves as a grade equivalent to the thickness which added the cap insulator layer 6 to the thickness of the gate electrode 5 For example, when thickness of 150 [nm] and the cap insulator layer 6 is set to 150 [nm] for the thickness of the gate electrode 5, As opposed to the amount of over etching permissible with the conventional technology serving as 150 [nm] grades equivalent to the thickness of the gate electrode 5 a book -- operation -- a gestalt -- **** -- the gate -- an electrode -- five -- the side -- a cap -- an insulator layer -- six -- receiving -- selectivity -- having -- etching -- a stopper -- a film -- ten -- covering -- having -- **** -- a sake -- being permissible -- over etching -- an amount -- the gate -- an electrode -- five -- thickness -- a cap -- an insulator layer -- six -- thickness -- having added -- thickness -- corresponding -- 300 -- [-- nm --] -- a grade --

[0070] next, the resist mask M2 -- removing -- the connection for after that and diffusion fields -- a hole -- inside and the connection for the gates -- by being filled up with electric conduction objects, such as a metal, forming the electric conduction plug 14 in a hole 13, and forming wiring 15 on the layer insulation film 11 after that, as shown in drawing 11 , the upper wiring 15 is electrically connected to MOSFETQ3

[0071] According to this operation gestalt, the following effects are acquired as explained above.

[0072] By forming the etching stopper film 10 which has selectivity to the cap insulator layer 6, after removing alternatively the sidewall spacer 8 formed in the side of the gate electrode 5 the contact for the gates from the gate electrode 5, when a hole 13 overflows Since the amount of over etching which can approve when **********ing the cap insulator layer 6 serves as a grade equivalent to the thickness which added the cap insulator layer 6 to the thickness of the gate electrode 5 the contact for the gates -- the gate electrode 5 of MOSFETQ3 and impurity diffusion field (7 9) which are produced through the electric conduction object (the electric conduction plug 14 or a part of wiring) with which it filled up in the hole 13 -- simplistic -- the receiving margin can be enlarged

[0073] moreover, the gate electrode 5 of MOSFETQ3 and an impurity diffusion field (7 9) -- simplistic -- since the receiving margin can be enlarged -- the element formation field top of the semiconductor substrate 1 -- setting -- the contact for the gates -- a hole 13 can be formed easily and detailed-ization of MOSFETQ3 can be attained

[0074] In addition, although this operation gestalt explained the example which formed the etching stopper film 10 by the silicon nitride film, since the etching stopper film 10 should just have selectivity to a cap insulator layer and a gate electrode at least, it is not limited to a silicon nitride film.

[0075] Moreover, although the operation gestalt 1 and the operation gestalt 2 explained the example using MOSFET of the LDD structure which formed the low concentration impurity

diffusion field by the ion implantation method, you may be MOSFET of the LDD structure which formed the sidewall spacer with which the impurity was introduced into the side of a gate electrode, diffused the impurity from this sidewall spacer and formed the low concentration impurity diffusion field.

[0076] Moreover, although the operation gestalt 1 and the operation gestalt 2 explained the example which used the n channel conductivity type MOSFET, you may be the p-channel conductivity type MOSFET.

[0077] Moreover, although the operation gestalt 1 and the operation gestalt 2 explained the example which used MOSFET, it is not limited to this but the thing which may be MISFET is undoubted. The gate insulator layer of MISFET is formed by the Si-O-N film which oxidized for example, the thermal oxidation film in N2O gas atmosphere. For example, hot carrier resistance of MISFET using the gate insulator layer which consists of this Si-O-N film improves.

[0078] As mentioned above, although invention made by this invention person was concretely explained based on the aforementioned operation gestalt, this invention of the ability to change variously in the range which is not limited to the aforementioned operation gestalt and does not deviate from the summary is natural.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS [Brief Description of the Drawings]
[Drawing 1] It is a cross section for explaining the manufacture method of the semiconductor integrated circuit equipment which is the operation gestalt 1 of this invention.
[Drawing 2] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 3] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 4] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 5] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 6] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 7] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 8] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 9] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 10] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 11] It is a cross section for explaining the manufacture method of the semiconductor integrated circuit equipment which is the operation gestalt 2 of this invention.
[Drawing 12] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 13] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 14] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 15] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 16] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.
[Drawing 17] It is a cross section for explaining the manufacture method of the aforementioned semiconductor integrated circuit equipment.

[Drawing 18] It is a cross section for explaining the conventional technology.
[Drawing 19] It is a cross section for explaining the conventional technology.
[Drawing 20] It is a cross section for explaining the conventional technology.
[Drawing 21] It is a cross section for explaining the conventional technology.
[Drawing 22] It is a cross section for explaining the conventional technology.
[Drawing 23] It is a cross section for explaining the conventional technology.
[Description of Notations]
1 [-- The insulator layer for isolation, 4 / -- Gate insulator layer,] -- A semiconductor substrate, 2 -- A slot, 3 5 [-- Low concentration impurity diffusion field,] -- A gate electrode, 6 -- A cap insulator layer, 7 8 [-- Etching stopper film,] -- A sidewall spacer, 9 -- A high concentration impurity diffusion field, 10 the contact for 11 -- layer insulation film and 12 -- diffusion fields -- the contact for a hole and 13 -- gates -- a hole, 14 -- electric conduction plug, and 15 -- wiring, M1, an M2 -- resist mask, Q1 and Q2, and Q3 --MOSFET

[Translation done.]

JAPANESE [JP,2000-091440,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS DESCRIPTION OF DRAWINGS DRAWINGS

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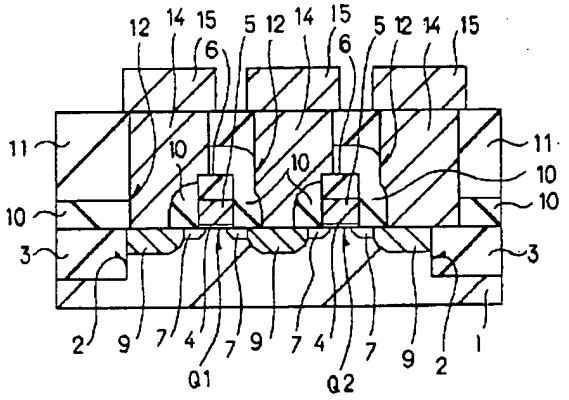
DRAWINGS

[Drawing 1]

図 1



[Drawing 2]

JAPANESE [JP,2000-091440,A]

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DRAWINGS

[Drawing 1]

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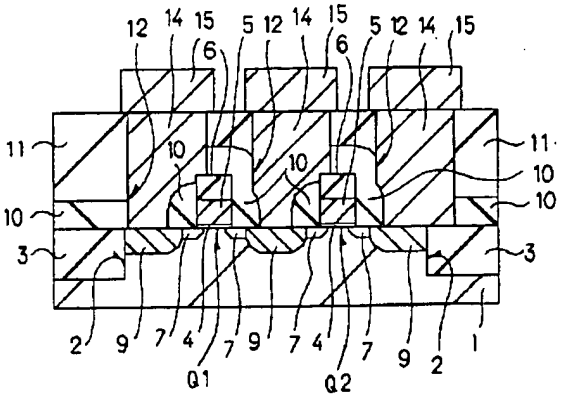
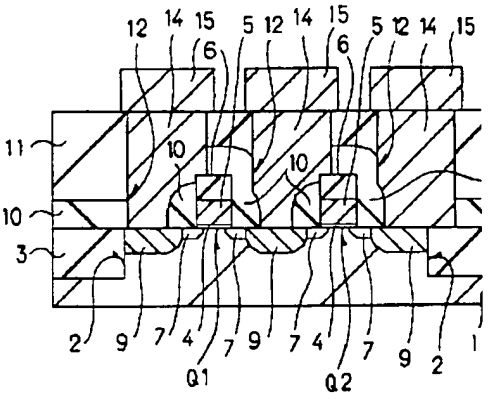


[Drawing 2]

Drawing selection

drawing 1

図 1



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JAPANESE [JP,2000-091440,A]

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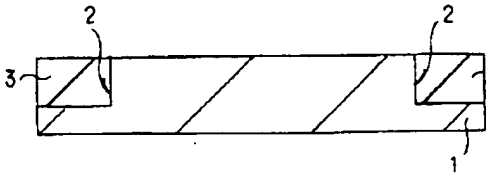
Drawing selection

drawing 2

図 2



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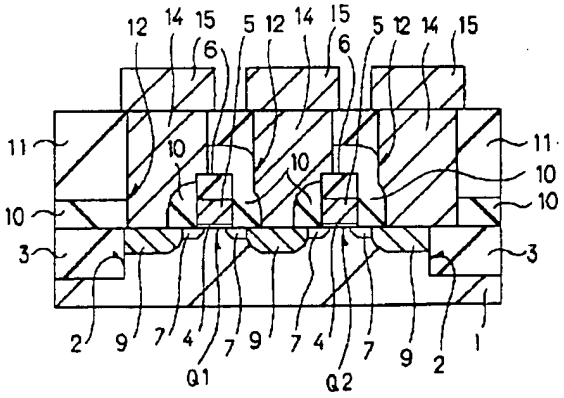
DRAWINGS

[Drawing 1]

図 1



[Drawing 2]

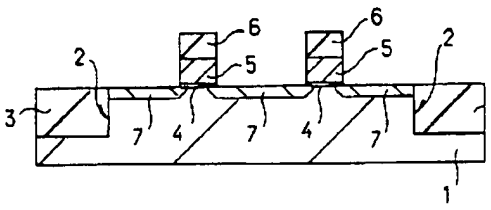
JAPANESE [JP,2000-091440,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS DESCRIPTION OF DRAWINGS DRAWINGS

Drawing selection

drawing 3

図 3



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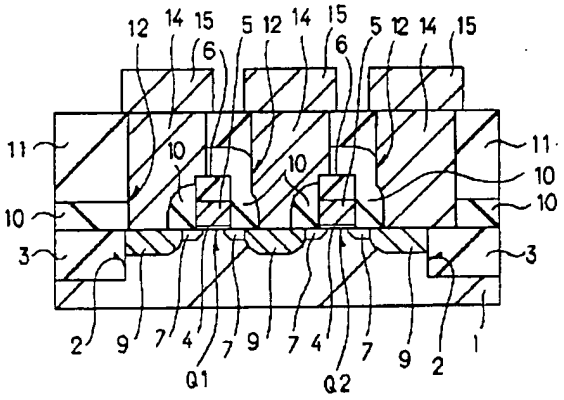
DRAWINGS

[Drawing 1]

図 1



[Drawing 2]

JAPANESE [JP,2000-091440,A]

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[Drawing 1]

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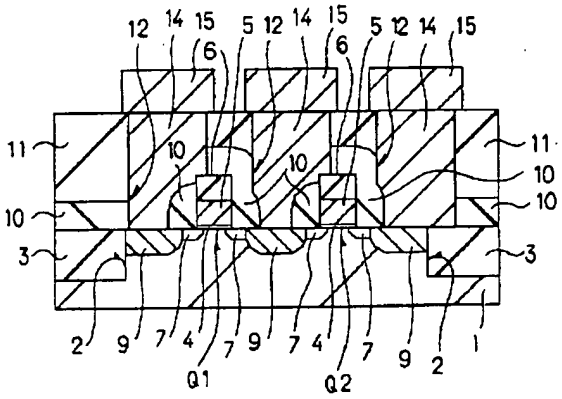
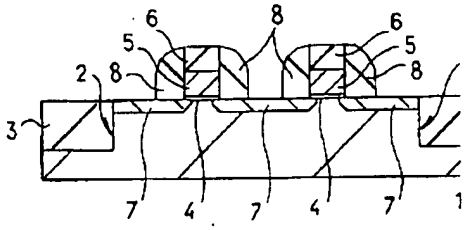


[Drawing 2]

Drawing selection

drawing 4

図 4



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[Drawing 1]

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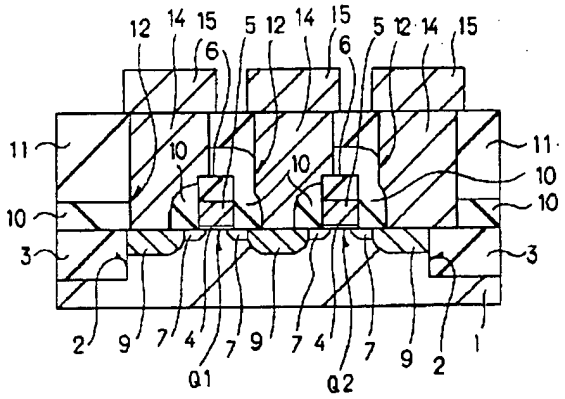
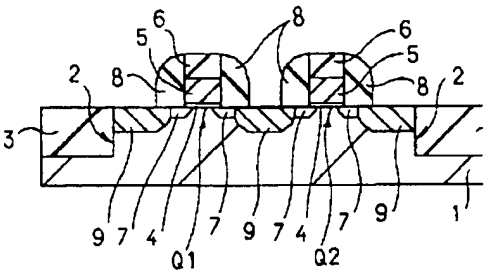


[Drawing 2]

Drawing selection

drawing 5

図 5



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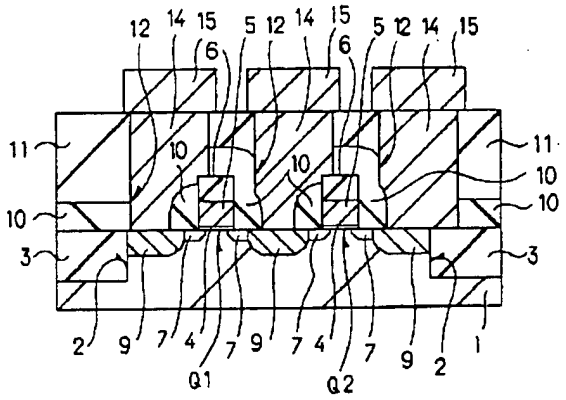
[Drawing 1]

図 1

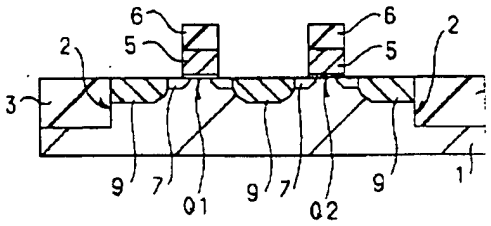


[Drawing 2]

Drawing selection

drawing 6

図 6



[Translation done.]

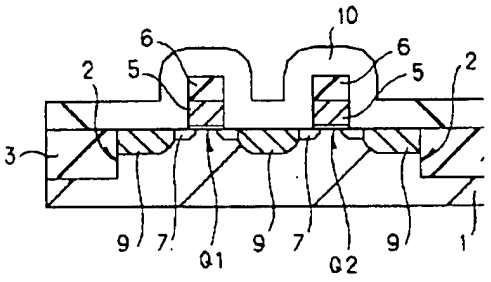
JAPANESE [JP,2000-091440,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS DESCRIPTION OF DRAWINGS DRAWINGS

Drawing selection

drawing 7

図 7



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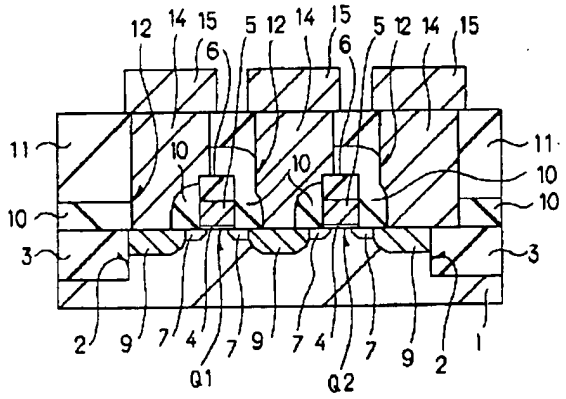
DRAWINGS

[Drawing 1]

図 1



[Drawing 2]

JAPANESE [JP,2000-091440,A]

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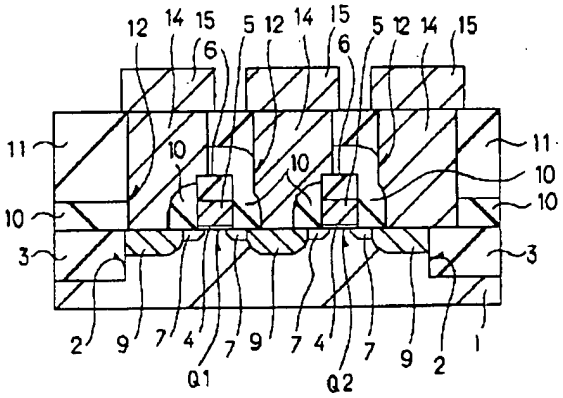
DRAWINGS

[Drawing 1]

図 1

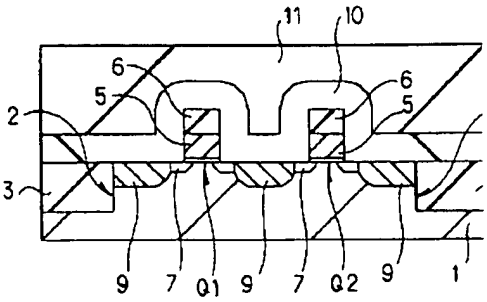


[Drawing 2]

Drawing selection

drawing 8

図 8



[Translation done.]

JAPANESE [JP,2000-091440,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS DESCRIPTION OF DRAWINGS DRAWINGS

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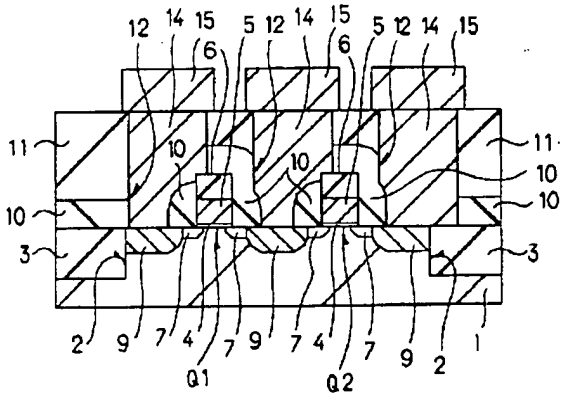
DRAWINGS

[Drawing 1]

図 1

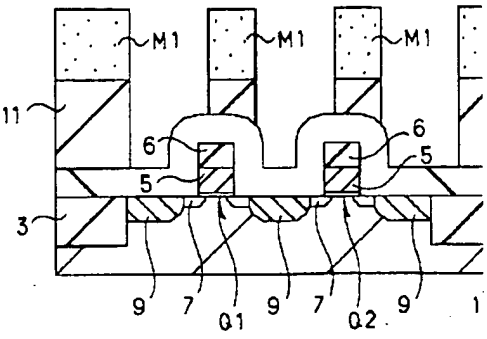


[Drawing 2]

Drawing selection

drawing 9

図 9



[Translation done.]

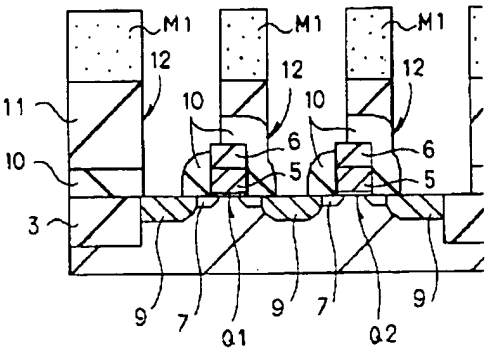
JAPANESE [JP,2000-091440,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS DESCRIPTION OF DRAWINGS DRAWINGS

Drawing selection

drawing 10

図１０



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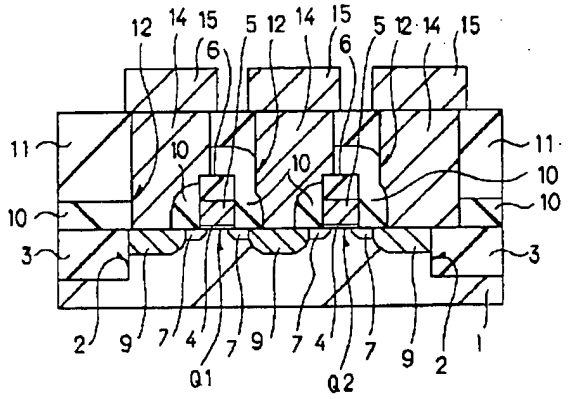
DRAWINGS

[Drawing 1]

図１



[Drawing 2]

JAPANESE [JP,2000-091440,A]

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DRAWINGS

[Drawing 1]

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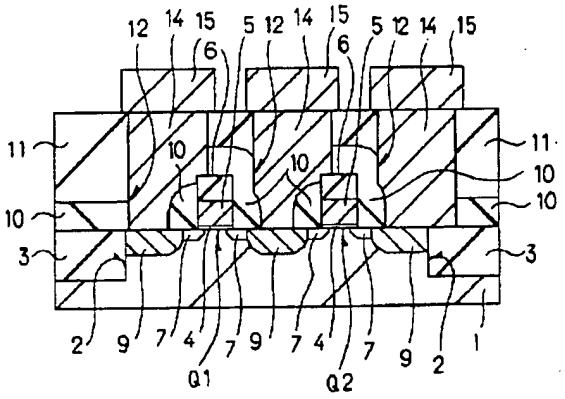
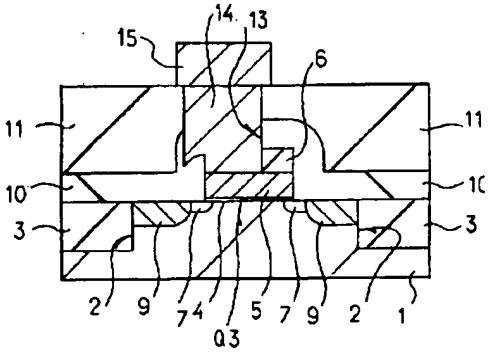


[Drawing 2]

Drawing selection

drawing 11

図 1 1



[Translation done.]

JAPANESE [JP,2000-091440,A]

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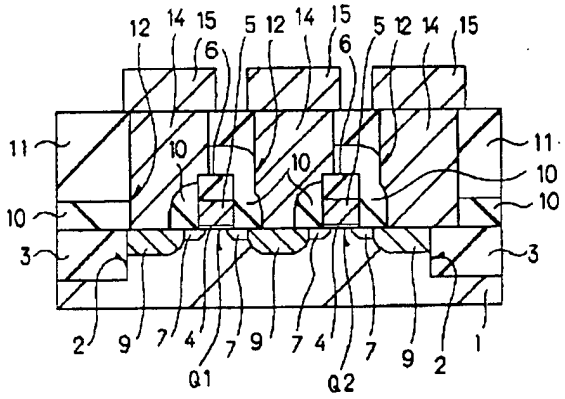
DRAWINGS

[Drawing 1]

図 1

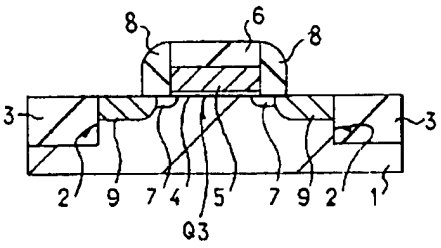


[Drawing 2]

Drawing selection

drawing 12

図 1 2



[Translation done.]

JAPANESE [JP,2000-091440,A]

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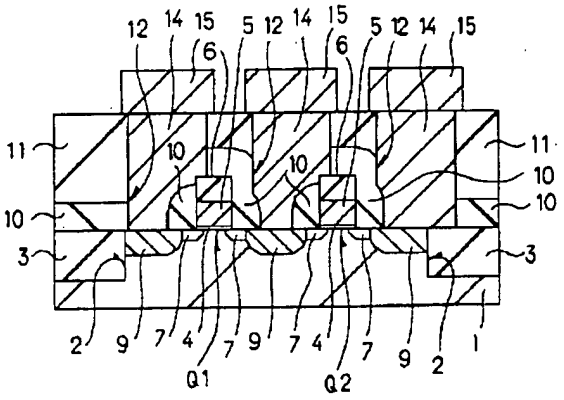
[Drawing 1]

図 1

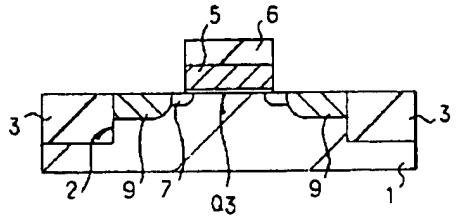


[Drawing 2]

Drawing selection

drawing 13

図 1 3



[Translation done.]

JAPANESE [JP,2000-091440,A]

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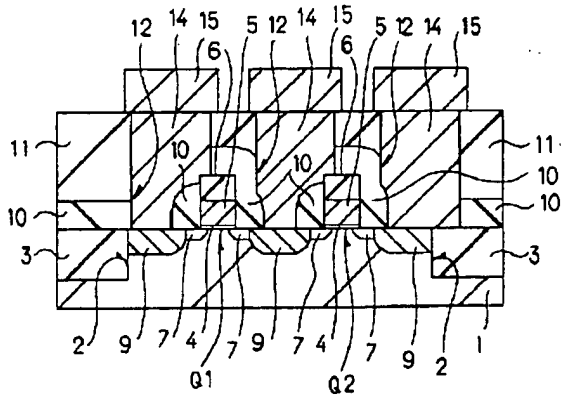
DRAWINGS

[Drawing 1]

図 1

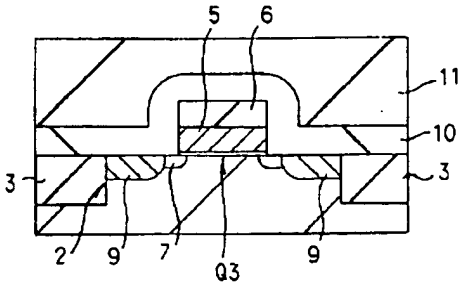


[Drawing 2]

Drawing selection

drawing 14

図 1 4



[Translation done.]

JAPANESE [JP,2000-091440,A]

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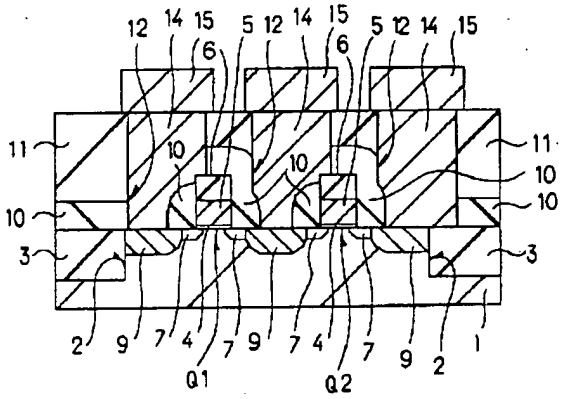
DRAWINGS

[Drawing 1]

図1

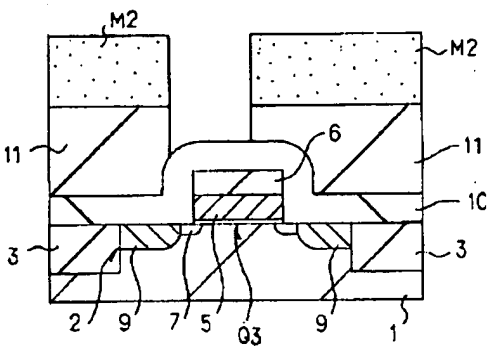


[Drawing 2]

Drawing selection

drawing 15

図15



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JAPANESE [JP,2000-091440,A]

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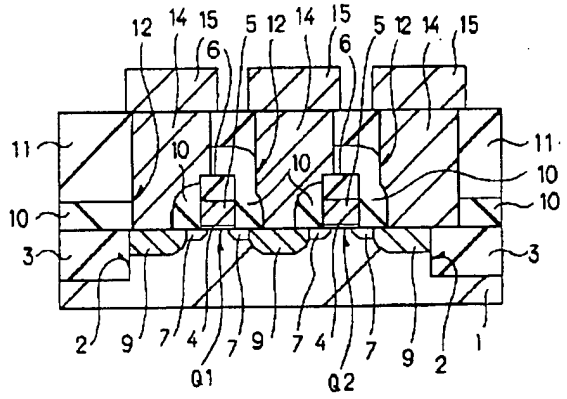
DRAWINGS

[Drawing 1]

図1

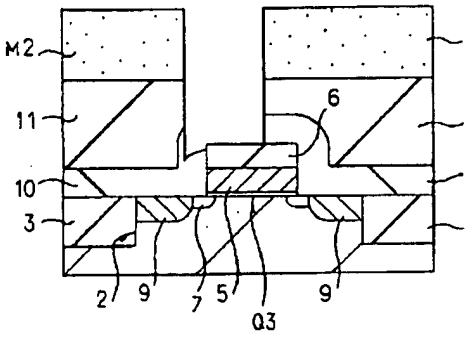


[Drawing 2]

Drawing selection

drawing 16

図16



[Translation done.]

JAPANESE [JP,2000-091440,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS DESCRIPTION OF DRAWINGS DRAWINGS

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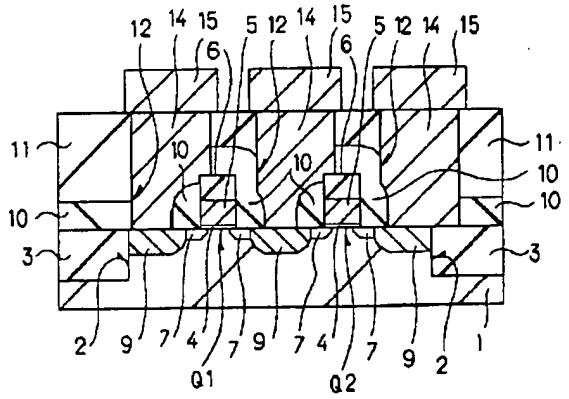
DRAWINGS

[Drawing 1]

図 1

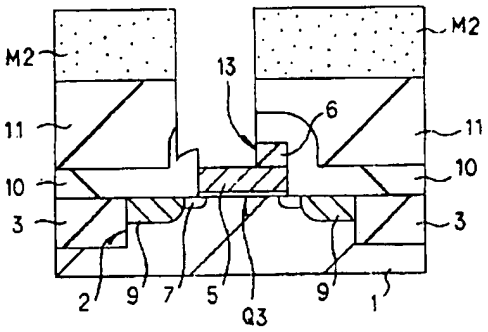


[Drawing 2]

Drawing selection

drawing 17

図 1 7



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JAPANESE [JP,2000-091440,A]

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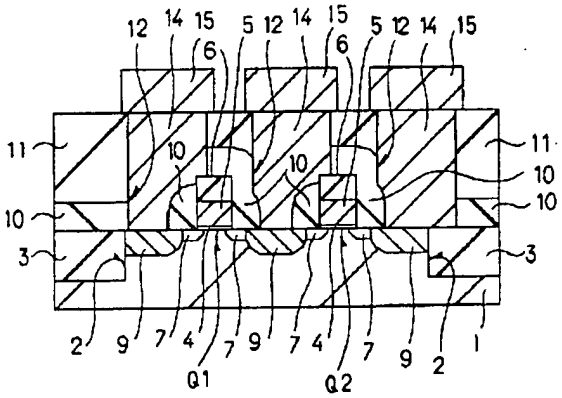
DRAWINGS

[Drawing 1]

図1

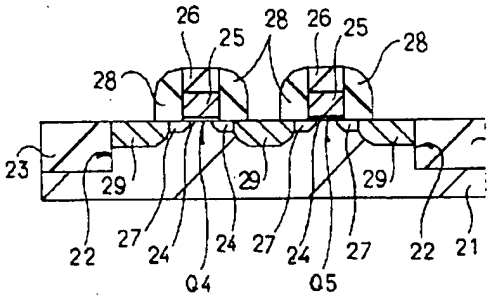


[Drawing 2]

Drawing selection

drawing 18

図18



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JAPANESE [JP,2000-091440,A]

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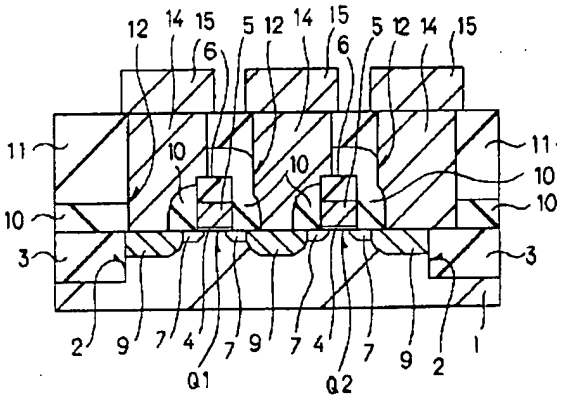
DRAWINGS

[Drawing 1]

図1

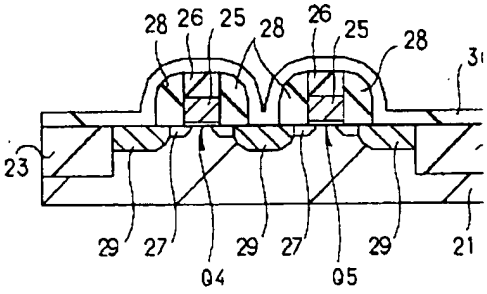


[Drawing 2]

Drawing selection

drawing 19

図19



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JAPANESE [JP,2000-091440,A]

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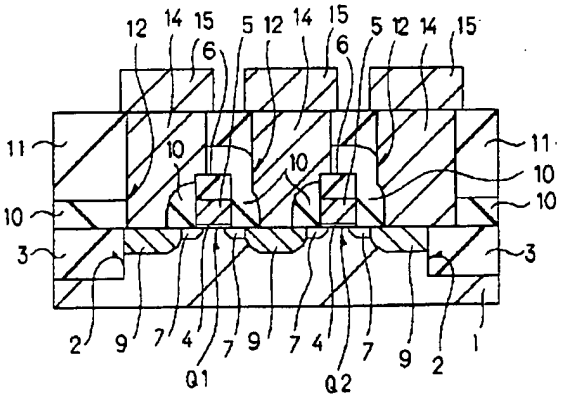
DRAWINGS

[Drawing 1]

図 1

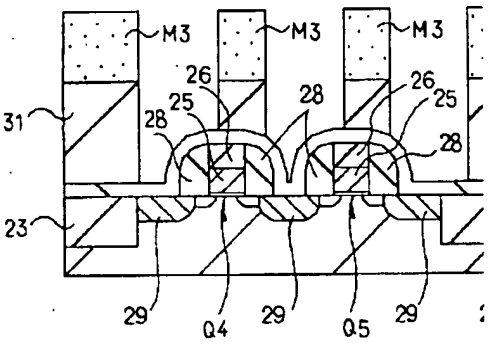


[Drawing 2]

Drawing selection

drawing 20

図 2 0



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JAPANESE [JP,2000-091440,A]

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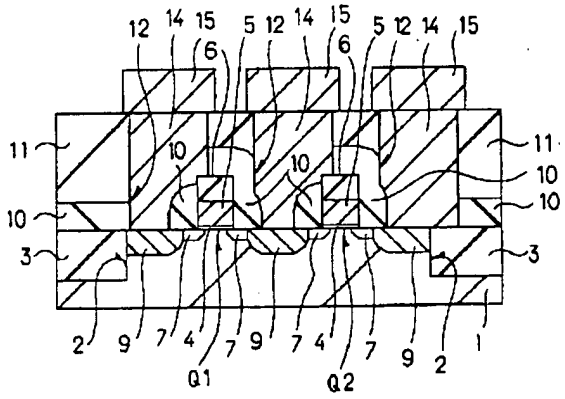
DRAWINGS

[Drawing 1]

図1

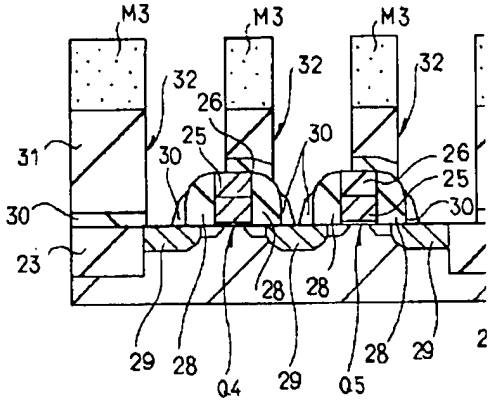


[Drawing 2]

Drawing selection

drawing 21

図21



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JAPANESE [JP,2000-091440,A]

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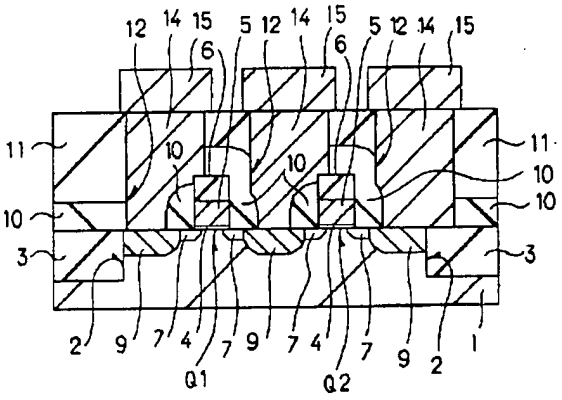
DRAWINGS

[Drawing 1]

図 1

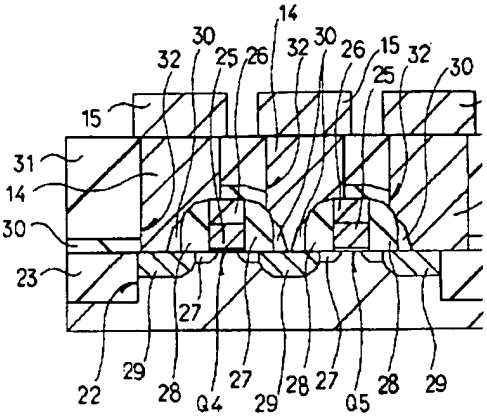


[Drawing 2]

Drawing selection

drawing 22

図 2 2



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JAPANESE [JP,2000-091440,A]

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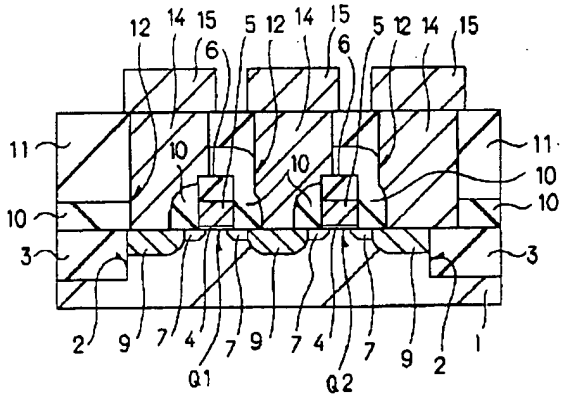
DRAWINGS

[Drawing 1]

図1

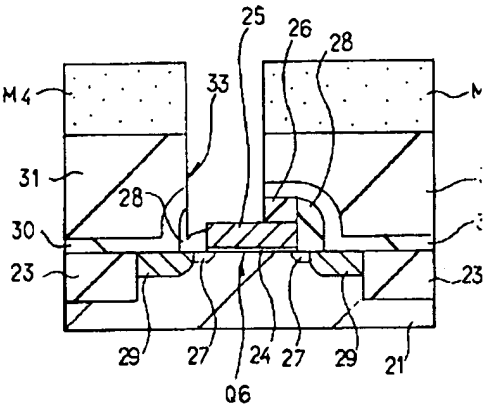


[Drawing 2]

Drawing selection

drawing 23

図2 3



[Translation done.]